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MODEL 8401-3 CONTROLLER MANUAL

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1.0 SCOPE

This manual, along with the associated literature, is intended to provide users of the 8401-3 Disc Drive Memory with complete information for the installation and maintenance of the equipment.

Specifically, this manual describes the installation of the controller and its cabling to the drive; the theory of operation of the controller and its maintenance; and aspects of the 5017-3 Disc Drive where relevant to the 8401-3 controller.

2,0 ASSOCIATED LITERATURE

In addition to this manual, the following items provide the complete documentation for the 8401-3 sub-system.

DS 8401-3	Specification	8401-3
DS 5017-3	"	5017-3
	Maintenance Manual	5017-3
	Test and utility software (see Appendix)	

3.0 INTRODUCTION

The 8401-3 Rotating Memory System, using up to two 5017-3 Disc Drives, provides a max. of 100 megabytes of on line storage to a DEC PDP11 computer.

Full details are provided in the specifications DS 8401-3 and DS 5017-3 which cover the overall 8401-3 performance and the 5017-3 Disc Drive respectively.

Briefly, the 8401-3 provides the necessary controlling registers, data buffering, drive addressing checks and an interface to the PDP11 UNIBUS and the 5017-3 Disc Drive. Various error conditions are monitered and reported along with controller and drive status through the device registers. Data transfers are performed by Direct Memory Access and Interrupts may be made to the processor on completion of data transfers, actuator movements or detection of error conditions.

4.0 SYSTEM INSTALLATION

CAUTION Before carrying out the installation work, consult the 5017-3 Disc Drive manual regarding all aspects of installing the disc drive/s.

4.1 INSTALLATION

The 8401-3 sub-system consists of a four slot backplane with d.c. power cable, four controller P.C.B.'s and one or two 5017-3 Disc Drives along with the necessary data/clock and control cables.

The backplane is physically DEC compatible and is screwed into a vacant space in the processor box or bus extender box of the user system.

See the Appendix for colours and connections of the d.c. cable which powers the controller boards from the processor PSU. The power requirements are as follows:-

+5V	4.5A
-15V	50mA
-5V	600mA

After installing the backplane and d.c. power cable, fit the four controller boards and UNIBUS jumpers/ terminator as shown in figure 1.

Connect the Control Cable (L16-S-0300-TAB) between board 2 (CP1 and CP2) and DP8 or DP9 on the drive.

If only one drive is connected, fit a control cable terminator into the vacant 75 way connector on the drive. In two drive applications, connect one end of the daisy chain control cable (L16 -S-0301-TAB) into this connector.

Fit the other end of the daisy chain cable into the second drive (DP8 or DP9) and the terminator in the vacant position.

The data/clock cable connections are made radially; that is to say, each drive has its own cable to the controller.

For each drive, therefore, connect a data/clock cable (L16-S-0299-TAB) between DP10 and CJ1 or CJ2.

Note: There is no distinction between CJ1 and CJ2 on board 3; the controller hardware determines where drive numbers Ø and 1 (as dialled on the drive thumbwheel switches) are connected.

Figure 2 details these cabling arrangements.

4.2 ADDRESS AND PRIORITY PATCHES

The standard version of the 8401-3 is built with the following patchable characteristics:-

UNIBUS address range occupied:-

776700 - 776736

(lowest register address VTDS is 776710)

VECTOR address: 254

Priority level: 5

If it is desired to alter any of these characteristics, the Appendix at the rear of the manual contains the relevant information.

4.3 OPERATION

When installation is completed, connect a.c. power to the drive/s and after ensuring that a cartridge is fitted in each, place the STOP/STANDBY/RUN switch in the STANDBY position. The drive/s will run up to normal operating speed but the heads will not load. Leave the drive/s in this state after first switch on, for about 15 minutes to thoroughly purge the head flying area.

Other than the few front panel lights and controls on the 5017-3, which are described in the 5017-3 manual, all system operation is via software control from the PDP11 processor.

However, correct operational status should be determined at this stage by running the test programmes shipped with the hardware.

The various software supplied is described in the Appendix. Briefly, the static tests check the various controller functions and the dynamic test checks the overall sub-system performance in storing and retrieving data.

Run both these programmes at this stage.

5.0 SECTOR FORMAT

Details regarding the disc storage area, generation of sector pulses and the role of the interspersed Servo data are given in the 5017-3 manual.

However, to understand the controller operation, as described in the next section, it is essential to be aware of how the controller groups disc sectors in pairs, and the concept of sector interlace and sector header data. These phenomena are explained in this section.

5.1 SECTOR INTERLACE AND GROUPING

Each 5017-3 disc is initialised with fifty sector marks per track. The gap between these sectors is sufficient for 256 bytes of data in addition to space for essential 'housekeeping' information. Since a sector size at the UNIBUS interface is defined as being 256 words, it is necessary to group two disc sectors together to produce the required size.

To achieve the specified average word transfer rate, it is necessary to handle alternate sectors to effectively halve the data rate of the drive. This constitutes sector interlacing and could be performed at UNIBUS sector level or disc drive sector level.

This sector interlacing is performed at drive sector level since this involves interlacing smaller sector sizes and hence halves the data buffering requirement. The final format of UNIBUS sectors appears in part as shown in figure 3.

From this, it can be seen that UNIBUS sector Ø (shown as ØA and ØB) consists of drive sectors Ø and 2 grouped together and UNIBUS sector 1 is drive sectors 4 and 6 grouped together and so on. The use of alternate drive sectors provides the 2:1 sector interlace.

It will also be seen that to transfer one whole track of data, it is necessary to complete two revolutions of the disc, i.e. UNIBUS sectors Ø

through 14A on the first revolution, 14B through 30 on the second.

A complete chart relating UNIBUS (controller) sectors to Drive sectors is shown in the Appendix. This can be of use if, for example, sectors 4 and 21 on a particular track show problems, when it will be seen that these use adjacent drive sectors 22 and 23.

From this point, the term 'sector' will be used to describe the UNIBUS 256 word sector. Drive sectors (256 bytes) will be referred to specifically by the term "Drive sector".

5.2 THE SECTOR HEADER

In order to verify both the positional accuracy of the actuator and the sector counter validity, the unique sector address is pre-recorded at the commencement of each drive sector in a separately addressable block known as the header. The actual construction of the header is shown in the Appendix. It consists of five 16 bit words: the first two form the mandatory header address field which contain the platter select bit, the track and sector address and other bits which will be explained later. The next two words are usable by the operational software if so desired. The final word is always transparent and is the cyclic redundancy check (CRC) word for the header. The use of the CRC is covered in the later section "Read operation".

The header information is generated within the controller at the start of each transfer at the same time as the pre-recorded header is read off the disc. The one is checked against the other and if there is no comparison error and no CRC error, the actual data transfer is allowed to proceed. This header check is performed for every drive sector transferred. The format on the disc therefore appears as shown in Figure 4.

6.0 THEORY OF OPERATION

Drawing conventions used in the logic diagrams are explained in the Appendix.

Reference will be made throughout this explanation to the System Arrangement/Block Diagram LI-0142 which, along with the logic diagrams, is located at the rear of the manual.

The block diagram shows the physical arrangement of the four controller boards in the backplane, the cabling for two drive working, and an overview of control logic and data flow represented within the appropriate board boundaries.

The main central feature of the controller is the use of an internal tristate data bus, shown in heavy lining, which carries both control and storage data to and from the UNIBUS. This is a sixteen bit highway and is identified in the logic diagrams with the signal names DBØ through DB15.

The UNIBUS connects with the controller at the left hand side of the drawing and the blocks on boards 2 and 3, over the UNIBUS area, represent line drivers or receivers.

6.1 DEVICE ADDRESSING

The 8401-3 is addressed by the current bus master in the same manner as any other UNIBUS peripheral, that is, by addressing one of the sixteen bus addresses occupied by the device. Ten of these are used by the 8401-3 as the addresses of its Device Registers and these, along with the Vector Address (referred to later), effectively define the identity of the 8401-3 on the UNIBUS.

These addresses are hardwired on 'patch' positions on the controller and the device identity can therefore be altered if desired by using the information given in the Appendix.

The eighteen UNIBUS address lines are monitored by the 8401-3 as represented in figure 5.

The block diagram shows the eighteen bus address lines received on board 2. The thirteen most significant of these are decoded in the device address logic on receipt of a MSYN signal from the bus. If an 8401-3 device register address is recognised, the register address decoder is enabled.

The logic diagram for board 2 shows eight of these address lines routed via the patch facility in position R1 which allows the device identity to be altered. Thereafter, Y3-3 level will be low when the 8401-3 recognises its address group. This, via T2, causes the timing components on R2 to produce SSYN which is sent to the UNIBUS in response to the MSYN received.

6.2 DEVICE REGISTERS

Device addressing as explained in the last section, will always be for the purpose of reading or loading one of the ten device registers. These registers are for defining the operation, and reporting the status of the sub-system. A detailed description of the device registers is given in the 8401-3 specification and a summary of their bit definitions is given in the register chart in the Appendix. Along with the register address, is sent a level on the C1 control line which determines the direction of data on the UNIBUS, i.e. in this case whether the addressed register is to be read or loaded.

The register address decoder, positions U2 and V2 generates a signal for the specific register addressed and the gates U1 and N2 produce a register loading pulse "REG STR" or a register reading pulse "REG OUT", respectively, depending on the level of the C1 control line.

In general the device registers are shown on the block diagram as in figure 6.

If C1 is active, i.e. low on the UNIBUS, REG STR is generated and the data on the data bus is loaded into the specified register.

If C1 is not active REG OUT is generated and the contents of the specified register are gated out via the tristate bus driver and the data bus.

Figure 7 shows the signals involved in loading and reading a register.

6.2.1. ZERO LINE FILL

As can be seen on the register chart in the Appendix, various bit positions are either not used or are 'write only' and in both cases when reading the relevant register these positions should return as zero.

The "Zero Line Fill" block on board 2 (LI-0142) performs this requirement. It consists of two programmable, read only memories (PROMS) which have their address inputs connected to the four least significant bus address lines (ignoring bit AØ). The PROM contents are therefore selected for each 8401-3 device register address. The enable input of the PROMS are connected to REG OUT, so that when any register is read by the processor, the PROMS output a specific pattern along with the specified register contents. The PROMS are blown so that any unused bit position for each register address will be zero and since the PROM types used are 'open collector' all other positions will not be affected.

6.3 ACTUATOR MOVEMENT

This section covers the operations "Restore" (home seek) and off line "Seek". The term "off line" is used since once the actuator movement is initiated, controller attention is not required and the processor can perform other tasks.

A seek operation is automatically performed with any transfer function so, operationally, off line seeks will only be performed for time optimisation of software and more probably where multiple drive operation is carried out.

6.3.1. SEEK OPERATION

BD1 To perform a seek operation, the Cylinder Address Register is first loaded with the relevant address.

BD2 The desired drive unit number and disc (upper or lower) are selected by setting the appropriate bits in the Control And Status Register along with the function bits for the seek operation. The "Go" bit is set at the same time or "bit set" in subsequently in order to initiate the operation. The controller is "not ready" for a period necessary to select the desired drive and start the seek operation. After that time (approximately 6μS) it will be free to accept another command from the processor.

The GO bit is temporarily stored in one-shot P2. This allows time to select the drive and perform an initial resetting operation.

Before commencing any operation with the disc drive, it is necessary to clear out any error conditions, which may have been set during a previous operation.

This is performed whenever the GO bit is loaded,

by H5 producing ERR CL through J3. ERR CL is delivered to all boards in the controller and via board 1 provides a reset signal to the drive.

When SSYN is generated GO DLY is clocked into Y2 so setting the I/O GO state. This clears RDY (U1-8) which enables the function decode chip L4.

The Control and Status Register (VTCS) consists mainly of counter P3 for the extended address bits and latches M4 and M5 for holding the function bits, disc and unit select bits, etc.

The seek function loaded into VTCS is now decoded by L4 to generate an active low output on pin 11 which sends DSEEK to board 1.

BD1

Control information for the drive is multiplexed on the BUSO lines and identified by sending one of the three TAG signals. These define BUSO information as follows:-

TAG 1 — BUSO Ø - BUSO 9 define the least significant ten lines of track address.

TAG 2 — BUSO 9 defines which disc, upper or lower is selected.

TAG 3 — BUSO 6 specifies a Restore operation
BUSO 4 specifies a reset operation
BUSO 1 specifies a read operation
BUSO Ø specifies a write operation.

Whenever a Seek operation is required, the controller always sends control information to the drive in the sequence TAG3, TAG2,TAG1.

The TAG3 information performs an initial drive reset, the TAG2 selects the upper or lower disc and the TAG1 loads the required track address and initiates the Seek operation.

The tag generator block (LI-0142) on board 1 performs this sequence and consists basically of a 7496 shift register in position C4.

Whenever a drive is selected, a local oscillator consisting of capacitor C4, resistor R3 and a Schmitt input nand gate D2 is allowed to free run. This has a period of approx. 300nS and is used to clock the shift register C4 which is configured as a ring counter to produce a series of active low timing pulses, T1(L) through T5(L).

The ring counter is only enabled by the logic function SEEK+RESTORE+RESET so that once a tag cycle has been completed, although the local oscillator is running for the entire period of selection, the tag generator shuts down.

The sequence of events for a seek operation, therefore, is shown in the timing diagram Figure 8.

The signal ERR CL from board 2 clocks flip flop D3 to latch DRESET. SELEN releases the local oscillator after the MASK one-shot on board 2 times out. This delay is to allow time for the drive selection to take place.

The quiescent state of A5-1, which is the enable signal for multiplexing control signals to the drive, is active (low) hence DRESET on A5-4 is gated out on to the BUS04 line. When the ring counter produces T2(L), TAG3 will be sent to the drive from B6-3. T5(L) subsequently clears DRESET.

DSEEK from board 2 latches SEEK in E3 and when DRESET is cleared F3-1 produces a clock edge to D6-11 to generate PLATT ENABLE. This enables the PLATT level on A5-12 to be gated out on the BUS09 line. C6-3 is also enabled such that T1(L) will produce TAG2. T4(L) on B5-5 will cause D6 to be preset so removing PLATT ENABLE.

At this time, C5-11 produces TA EN(L) which gates some of the track address lines to the drive and enables C6-4 to send TAG1 at T1(L) time. At the following T3(L) time, F3-4 will clear the SEEK condition from E3.

With the clearing of DRESET and SEEK, SEEK+RESTORE+RESET changes to the inactive state and presets the ring counter to its quiescent condition so

shutting off timing pulse generation.

BD2

During the period of tag generation described above, I/OGO on board 2 remains active and maintains the controller 'not ready' status.

The removal of SEEK+RESTORE+RESET (S+R+R) informs board 2 that the seek operation has been initiated such that the controller can relinquish control. J1 will go low and when H2-11 subsequently goes high, SELEN is reset so deselecting the drive.

J2 is clocked by the trailing edge of S+R+R signal and providing no transfer function was requested, i.e. K5-4 is high, J2-6 delivers a low level to Y1-1 to reset I/O GO via X1.

This sets the RDY state (U1-8) and completes the controller involvement in the seek operation until the actuator positions the heads at the desired cylinder address.

6.3.1.1. ATTENTION LOGIC

It is the function of the attention logic to report to the processor when a drive has completed a seek or restore operation.

Since either of two drives connected to the controller could be identified as unit Ø or I it is also necessary for the attention logic to ascertain which drive is responding with the SEEK COMPLETE signal.

The unidentified drives are referred to as A and B and the signals SCA, SCB, ASELD and BSELD refer to these drives.

The way in which this logic works is as follows:-

Assume that when an off line seek operation is initiated on drive Ø, drive A responds with ASELD on the D inputs of both halves of flip flop D4. As drive Ø was selected, at the end of the selection period during which the seek is initiated, a rising edge will appear from F5-11. This clocks C4-3 and D4-3 and as BSELD is not active, only D4-5 will switch to enable B4-10.

This condition is latched after the drive is deselected such that when drive A completes its seek operation and SCA (SEEK COMPLETE A) is received, ATTENTION Ø is generated by B4-8.

Reference to the logic diagram will show that had drive B responded instead of A, C4-5 would have latched to produce ATTENTION Ø via B4-3.

Either attention bit setting causes E4-6 to produce the signal ATTENTION which is used internally to generate attention interrupts.

The specification of the system states that an attention bit may be selectively cleared by loading the same bit into the Device Status Register (VTDS). This facility is accomplished by directing the appropriate bits DBØ or DB1 gated with the Status Register strobe from D5-3 to the reset inputs of the relevant flip flops C4 and D4

6.3.2 RESTORE (HOME SEEK)

This is handled by board 2 in the same manner as is a seek operation except that the signal DRESTORE(L) is produced.

BD1 Board 1 receives ERR CL(L) and DRESTORE(L) and latches DRESET and RESTORE respectively.

The drive electronics always selects head 1 after a restore since a restore is basically a heads unload, heads load sequence. It is therefore meaningless to select the upper or lower disc when performing this operation.

As there is no disc select or seek involved, TAG2 and TAG1 are not needed. The sequence of events is shown in figure 9 and is as follows:-

The operation is the same as for a seek up to completion of the drive reset. Thereafter, as PLATT ENABLE is not switched and TA EN not generated, the removal of DRESET will replace BUS04 with BUS06 and the next cycle of the ring counter will cause T2(L) to generate a second TAG3. The following T4(L) will reset RESTORE, shut down the ring counter and remove SEEK+RESTORE+RESET so terminating controller action on board 2 as for the seek operation. On completion of the restore, the attention logic will function as described in section 6.3.1.1.

6.4 DATA TRANSFERS

This section covers an explanation of all the controller functions:- Write Data, Read Data, Write Check Data, Write Header (Format) and Read Header (Maintenance).

It should be noted that all these operations incorporate an automatic seek to the specified track and that therefore a preliminary seek operation is not necessary. This automatic seek is performed in the same way as an off line seek and as such is explained in section 6.3.1.

For reasons of data security, before any data transfer is made, the header of the desired sector is read from the disc and checked for validity. Section 5.2 gives details about the sector header and its format is shown in the Appendix. Section 6.4.2. explains how the controller logic generates and checks the sector headers.

6.4.1. DIRECT MEMORY ACCESS (DMA)

All storage data to and from the 8401-3 is transferred by DMA operation with the UNIBUS.

It is assumed that service personnel working in this area have an understanding of how the UNIBUS operates in this respect.

BD2 Before a data transfer is started, all the relevant Device Registers will be loaded by the software to define the storage area on the disc, length and type of transfer, and the UNIBUS address where the transfer is to commence.

The Word Count Register (VTWC) on board 2 is loaded with the two's complement of the number of words to be transferred and defines how many 'handshake' cycles the DMA logic will make before communication with the UNIBUS is terminated. (The Drive Word Count Register - VTDWC controls communication between the controller and the drive. This is explained in section 6.4.3.2.)

The Bus Address Register (VTBA) consisting of K3, L3, M3 and N3 is loaded with the least significant fifteen bits of bus address information (A1-A15). The two remaining bits A16 and A17 are the extended address bits which must be loaded through VTCS. AØ is not used since all data transfers are word orientated and therefore use even numbered bus addresses.

The output lines (A1BØ - A17BO) from this register are connected to the bus address drivers S5, T5, U5, T2 and T4. These are gated by the DMA signal NPMSTR2.

BD3 Requirement for a DMA cycle during write operations arises when the Bus I/P Buffer (LI-0142) indicates 'empty' status. This is flagged by flip flop K1 asserting MT1.

MT1 (H) on U3-1 causes NPR to be produced at X2-1. This initiates a DMA sequence by sending NON PROCESSOR REQUEST to the UNIBUS.

Logic on board 3 handles NPG from the UNIBUS to produce SACK and establish final ownership of the UNIBUS as per the usual requirements. Possession of the bus for DMA purpose is signified by the assertion of NPMSTR which transmits BBSY to the UNIBUS.

BD2 NPMSTR is delivered to board 2 as NPMSTR2 where it gates the bus address driver as mentioned previously and in this case, the bus data receivers W4, X4, and Y4, via gates J4 and S2.

BD3 After asserting NPMSTR, if previous activity on the UNIBUS has completed, SSYNI (L) on T1-2 will be high so that one shot T1 will produce MSYN WAIT. This in turn fires the other half of T1 to produce a nominal 20 μS timeout period explained later.

On completion of MSYN WAIT (nominal 150nS), U2 will be clocked to assert MSYN on the UNIBUS. If the bus address transmitted is recognised, SSYNI will appear on V1-2 to trigger one-shot S1. If SSYNI does not appear within the timeout period referred to previously, U2-11 will be clocked to produce the error condition NON EXIST MEM (NEM). This produces an alternative trigger level at S1-1 to continue the bus cycle to completion and avoid a 'hang up' condition.

After triggering S1, pin 13 provides a nominal 75 nS de-skew period before firing the other half of S1 to generate TED (Tail End De-skew).

At this time, the data from the UNIBUS is active on the internal data bus and is strobed into the Bus I/P Buffer (M4, N4, P4 and R4) by TED on N1-5. This also clocks K1 on pin 3 to change the status MT1 to inactive, indicating that the Bus I/P Buffer is full.

TED (L) on U2-1 removes MSYN. and via V2-3 and W1-1 resets NPMSTR after 75 nS when it expires.
The negation of NPMSTR removes BBSY which signifies the end of the DMA cycle and relinquishes possession of the UNIBUS.

BD2 TED is used on board 2 to increment the Word Count Register once for each DMA, and when this eventually overflows, I/O OVFL will terminate the transfer and the BUS Address Register will point to the next bus address after the transferred block.

6.4.1.2. READ OPERATION DMA

BD3 DMA cycles during a read operation follow fundamentally the same sequence as for a write operation.

In this case, the Bus O/P Buffer initiates the DMA when its status flag MT2 (K2) goes inactive indicating that the buffer has a word of data to transfer to the UNIBUS.

MT2 (L) on U3-4 causes NPR to be issued to the bus so commencing the cycle.

NPMSTR is established in the same manner as for a write operation and as before, this is followed after 150nS by the assertion of MSYN by U2.

A read operation DMA follows the rules for a DATO since the 8401-3 becomes the bus master sending data to another bus address. Because of this, the de-skewing period provided by S1-13 during a write DMA, is not required, so this signal resets itself via W1 immediately it is generated.

The remainder of the cycle is the same as for a write operation except that in this case the bus drivers rather than receivers are enabled and the instigating signal MT2 is clocked to the active state indicating Bus O/P Buffer empty on the trailing edge of MSYNo.

6.4.2. HEADER GENERATION AND CHECKING

The data area in every drive sector is pre-formatted with header information as described in section 5.2. This header data is generated by the controller hardware in order to perform the formatting operation and to check the sector header whenever a transfer is required.

Reference to LI-0142 will show the Header Generator on board 1. This assembles track and sector address information from the relevant registers and includes certain information from the Control and Status Register on board 2, viz. upper/lower disc and whether the sector addressed is to be marked as "bad" or "write protected". (These two facilities are explained in DS8401-3 and referred to below in sections 6.4.2.1 and 6.4.2.2).

The assembled header data is clocked out of the Header Generator at the appropriate time and delivered to board 4 where it is either sent to the drive (along with a CRC word) when formatting, or checked against the pre-formatted header on the disc, when requiring to do a data transfer.

Formatting requires two words of user data per header and these will normally be zero after a factory format operation.

The two user words may be recovered by performing a Read Header operation, specifying a word count of two for every header transferred.

In addition, a maintenance mode is provided which enables all of the header words (except the CRC word) to be transferred to the processor for checking purposes. This is accomplished by setting bit 12 (Read All) in VTCS along with the function bits for a Read Header operation. It is necessary to specify a word count of four for each header in this case, in order to transfer the two extra mandatory header address words.

6.4.2.1. HEADER WRITING

BD1 The Header Generator on board 1 consists of four eight bit shift registers in positions L3, L4, L5 and L6. In addition to track and sector address information on the parallel inputs, SWP (Set Write Protect), SBS (Set Bad Sector) and PLATT (H) are provided from Control and Status Register bit positions on board 2.

SECT B on L5-5 differentiates between the two drive sectors which make up the UNIBUS sector. When active, the second drive sector is specified.

A sector found to be poor in terms of data recovery may be marked "bad" by re-writing its header and setting the SBS bit (bit 11) in VTCS. This bit is brought to L5-2 and appears in the header written to the disc. The manner in which it is handled is described in 6.4.2.2.

Similarly, an individual sector may be protected against overwriting by setting the SWP bit (bit 14) in VTCS. The parallel input data is loaded into the Header Generator by HDR LOAD (L). At the start of the relevant sector when Read/Write clock pulses are received from the drive, the header information is clocked serially out to board 4.

BD4 The header data is routed on board 4 through A3-5 and D5-13 to C5-2. C5-6 produces serial WR DATA which is delivered to the drive via board 3 and the Data/Clock cable.

While the header data is being clocked out to the drive it is also routed via C5-1 and D5-11 to the CRC Generator B5. This accumulates a CRC word which is gated out at PARITY GATE time on to the WR DATA line, via C5-5, immediately after the header data is written.

6.4.2.2. HEADER READING

Headers will be read off the disc either automatically at the start of every sector transferred or under software control when the header data will be transferred to the processor.

In the first case the operation is invisible to the processor but otherwise the two cases follow largely the same course.

whenever a header is read, the header generator on board 1 produces serial header data as described in 6.4.2.1. and passes this to board 4 for header checking.

BD4 Header data from the drive appears on board 4 on the line SERIAL RD DATA. This is connected to J2-4 to compare with internally generated header data on J2-5. J2-6 will be a low level when the two inputs are equal. However, as the two input signals will not coincide exactly, the output is checked by a suitably positioned clock edge on flip flop E1. A4-8 supplies a clock, masked by A4-9 and A4-10 to check only the sector portion of the header, while the clock on E1-11 is similarly masked to check the track address and platter select bit. A further mask is applied to H2-13 to inhibit comparison checks on the positions of the write protect and bad sector status bits since these may appear in the read header but will not be present in the generated header during a header check operation. The 'bad sector' and 'Write Protected' status bits are examined by other logic on board 4. SERIAL RD DATA is also taken to B2-9 and C2-13, the other inputs of which are conditioned to mask the WP and BS conditions respectively. If discovered, C1-5 and C1-9, respectively, will latch in the low state, and if a data transfer using the current sector is attempted, B1-5 will latch the error condition BAD SECT VIOLATION, for read or write transfers, and B1-9 will latch WLO VIOLATION, for write transfers only.

The two error conditions, SECTOR HDR ERR and TRK/PLATT HDR ERR from E1-6 and E1-8 respectively, are taken to board 1 for certain error processing.

SERIAL RD DATA is also connected to pin 4 of R4 which is the least significant position of the SER/DES (Serialiser/De-serialiser) consisting of R4, P4, N4 and M4 (See also L1-0142).

The serial header data from the drive is clocked into

the SER/DES and if a read header operation has been instructed, HDR OP (H) on L1-8 will allow parallel data to be transmitted back to the processor.

Details of data flow (write and read) are given in the subsequent sections covering read data and write data operations.

In a maintenance read header operation, RD ALL (H) will be applied to N1-4 which will enable the Drive O/P Buffer status flag to operate for the two mandatory header address words, thus allowing them to be sent to the processor prior to the two user data words.

The last word of the header is the CRC word. The complete header from the drive is routed to B5-11 via C5-1 and D5-11. B5, the CRC generator/checker, generates for the header, a CRC word which should be identical to the CRC word clocked in to B5-11 during PARITY GATE time. If the CRC generator/checker confirms this, B5-13 will switch low on the last clock edge.

If B5-13 remains high after the last clock edge, C3-12 will be clocked to produce HDR CRC ERR which is taken to board 1.

BD1

All potential errors associated with a header read operation are saved until the end of the header field before ERR STAT is generated. This allows the header transfer to complete so that all error information is available to the processor for error handling.

If, for example, a track header error occurs and this is allowed to abort the transfer, it would prevent the CRC word from being checked. The header error could thus have been caused by a failure to retrieve the header correctly, rather than a failure in positioning the head actuator.

B6-6 on board 1 produces HDR ERR (H) which is strobed into D6 by the trailing edge of GO(L) i.e. at the end of the header transfer. This, along with HDR CRC ERR will generate ERRS 1 (L) at A4-3. ERRS1 is one of three possible sources of ERR STAT in VTCS (bit 15).

MNT RD HDR OP on B6-12 inhibits ERRS1 so that in the event of an error condition arising during this mode of transfer, all the header words can be transferred to the processor for checking purposes.

6.4.3. WRITE DATA OPERATION

The block diagram L1-0142 shows the data path for write and read operations. In the case of write transfers, the black arrows show how data appears on the tristate bus and is directed to the Bus I/P Buffer, through the 128 word Silo Block to the Drive I/P Buffer and thence to the SER/DES (Serialiser/Deserialiser).

The SER/DES converts the data to bit serial form which is clocked out to the disc drive when the correct sector is identified.

6.4.3.1. WRITE DATA FLOW

BD3 Following a DMA during the write operation the Bus I/P Buffer contains a word of data and its status flag MT1 will be inactive.

Providing all the silos H4, J4, K4 and L4 have their inputs ready, i.e. IR1 through IR4 are high, MT1 on N1-9 will cause the latch formed by L2 and J2 to generate SI (H). This clocks the data into the silo block.

Once in the silo, data is automatically rippled through to the output, causing the various silo O.R. status lines to switch.

When all four lines OR1 through OR4 indicate that data is available on the silo outputs, J1-8 goes low.

BD4 Data from board 3 is routed to the Drive I/P Buffer on board 4.

As soon as a write operation is acknowledged by board 4, as indicated by K2-9 being low, J3-8 sends a high level to board 3 to indicate I/P BUFF RDY.

BD3 I/P BUFF RDY on L2-4 allows DATA STR to be sent to board 4 to clock the silo output data into the Drive I/P Buffer. Also, J1-1 generates STRACK to increment the Drive Word Count Register.

BD4 When DATA STR appears on BD4, the data on the lines PDØ through PD15 is strobed into the Drive I/P Buffer consisting of N5, P5 and R5. The high level on R5/13 is also clocked through R5 to produce a high level on K2-11 which removes I/P BUFF RDY.

The data for writing to the disc, only progresses this far until the sector, to which the transfer is to be made, is accessed. When this occurs, and after the header is checked, LOAD SERDES (L) from M1-8 allows the first R/W CLK pulse in the data field to load the data from the

Drive I/P Buffer to the SER/DES. As soon as this is achieved, the first bit in the serial data stream is available at M4-11. Thereafter, successive R/W CLK pulses shift out the serial write data to board 3 via the following element output pins:- A3-6, D5-12 and C5-6.

Board 3 contains the line transmitter which drives data via the Data/Clock Cable to the 5017-3.

6.4.3.2 WRITE CONTROL LOGIC

BD2 After loading the various device registers with control and address information relating to the transfer, setting function code 2 (bit 1) along with the GO bit in VTCS will initiate a write operation.

Logic elements connected to L4, analyse the transfer requirement and, in this case cause H2-6 and J3-6 to produce DATA OP and WR OP respectively. These signals control logic on board 4 to handle the drive transfer accordingly.

L4-14 switched to the active low state to indicate a write function, and this produces an active level at K5-4 which goes low for any transfer function. H5 propagates this active state to generate DSEEK (L) which starts the automatic seek as described in section 6.3.1.

The level change on K5-4 clocks F5 to the other state, producing a latched low level on K5-3. When the initial seek has been started and S+R+R on K5-2 goes low, the signal XFER GO will be transmitted to board 3.

BD3 Board 3 contains the Drive Word Count Register (M3, N3, P3 and R3) which increments during a data transfer for every word of data passing to or from the disc drive.

This is necessary because when DMA cycles have been finished during a write operation, data will have been accumulated in the silo buffer waiting to be transferred to the disc. The drive end of the controller is therefore still busy until such time as this data has been written.

Similarly, in a read operation, when the required number of words has been recovered from the disc and the drive transfer terminated, there will still be data in the buffer waiting to be transmitted to the UNIBUS. The processor end of the controller is therefore still busy until the buffer has emptied.

The Word Count Register (VTWC) is used to terminate DMA operations and the Drive Word Count Register (VTDWC) to terminate drive transfers. Whenever VTWC is loaded, VTDWC is loaded

automatically with the same value. VTDWC may be loaded and read separately for maintenance purposes.

Board 3 also generates the signal RUN which is used on board 4 for controlling the drive transfer. XFER GO latches RUN until such time as the drive has transferred the correct number of words and the low going level from M3-12 clocks P1-3 to produce a reset on P1-13.

BD1 In addition to track addressing, which is covered in section 6.3.1, board 1 also handles sector addressing.

Having addressed the desired track and performed the necessary seek operation, it is now necessary to identify the correct drive sector to which the data is to be written.

The sector address has previously been loaded into the Sector Address Register (VTSA) N6 and P6.

The drive keeps a record of the drive sector currently under the write/read heads by updating the sector counter on its I/O interface board every sector pulse time.

The values in VTSA and the drive sector counter will be related as shown in the chart in the Appendix.

The sector counter value is converted by H6 and J6 to the same format as is held by VTSA. J6 and H6 are PROMS which use the drive sector counter contents as their address and produce a converted value which allows for sector grouping and interlace as explained in section 5.0.

The output from H6 and J6 is compared with the contents of VTSA by H5 and J5 when SEVA (Sector Valid) is active on H5-3. The A or B half of the sector is recognised by Sect B wired to J5-1.

A further security in the check is provided by ensuring the heads are ONTRK as seen by J5-14.

When these conditions are found, E5-8 produces SECT COMP (L) which is used by board 4 to start the header check operation.

BD4 When RUN is received by board 4 from board 3, it immediately sets the state BUSY at N2. No further action takes place until SECT COMP appears from board 1.

The sequence of events is shown in figure 10. BUSY removes the reset level from K1 such that when SECT COMP goes active

on F2-2, as long as a word of data is present in the Drive I/P Buffer as indicated by I/P BUFF MT, K1-3 will be clocked by SOS (Start of Sector) to give GO.

Before any data transfer is commenced, the header must be checked.

HDR ADDR FLD is activated by SOS(L) on D1-10 and this in turn, presets HDR FLD at H1-5.

Since a header check necessitates reading data from the disc, SOS(L) sets the condition SET RD at P2-11, and this along with GO produces RD ENB on M2-8 and RDENA on F2-13 which is sent to board 1 where it sends RD GATE and TAG3 to the drive.

GO turning on will set INIT LD (K1-8) which, with HDR ADDR FLD produces HDR LD from E5-6. HDR LD loads the relevant data into the Header Generator on board 1 and initiates GAP on board 4. GAP, which only appears for data operations, is a time slot, measured out by master clock (MCLK) pulses, in which the header field resides. GAP, effectively, is an extended sector pulse which masks out the header field and provides an edge for starting the subsequent DATA FLD.

RD GATE causes the selected drive to send data and read clock pulses from the current sector. The data received will be the sector header and this is checked as detailed in section 6.4.2.2.

Since HDR OP is not active on L1-8, the Drive O/P Buffer will not be able to ship data to the Silo Buffer. INIT LD also presets the Bit Counter F3 via F2-8. Bit 8 output (F3-11) immediately resets INIT LD.

The R/W CLK pulses received from the drive along with header data, increment the Bit Counter which is configured to produce a pulse from pin 15 every byte time. These pulses increment the Byte Counter E3, E4 to produce timing periods B1, B2, etc.

B1, along with an output pulse from the Bit Counter, causes one shot J4 to trigger and generate EOW PLS (End of Word Pulse) every sixteen bits.

B7, during HDR FLD, causes the D input of N1 (pin 12) to set N1-9 high on the trailing edge of the next EOW PLS. This provides the time frame PARITY GATE during which the header CRC word is checked.

B8 and B1 produce 9 EOW PLS at D3-10 which, during HDR FLD,

resets GO via H3-8.

Shortly after the header check terminates, assuming no errors arise, divided down master clock pulses at D2-4 will result in a low going pulse from D2-13 which terminates the time period GAP and produces DFP (Data Field Pulse) from A6-10. The trailing edge of GAP clocks D1-3 to turn on DATA FLD.

DFP through L2-1 switches off the SET RD state and so provides an enable to M2-2.

DFP also turns GO on again via F2-5, and this generates WREN B on M2-3.

M2-11 (WREN A) enables TAG3 and BUSOØ to be sent to the drive from board 1.

On receipt of R/W CLK, data is shifted out to the drive as explained in the last sub-section.

Timings from the Byte Counter control the operation, and when B255 appears on L5-2, PARITY GATE is turned on by the following EOW PLS.

As for a header writing operation (Section 6.4.2.1.), the serial data is also clocked into the CRC generator, B5. When PARITY GATE appears on E5-10, the generated CRC word is shifted out at B5-12 and appended to the serial data stream.

Following this, GO is reset by 257 EOW PLS (L) on E2-1. This same timing pulse on H3-12 sends INC SECTOR, via E5-3 to board 1, to advance the sector address in preparation for the transfer to the following sector. In the event of an error occurring, the transfer will have been aborted such that this signal will not be produced. The Sector Address Register will thus point to the sector at which the error occurred.

The drive write operation finishes at the end of the drive sector in which VTDWC overflows and resets RUN. Removal of RUN causes the preset N2-4 to go high such that when GO is switched off, at the completion of the UNIBUS sector, N2-3 will see a rising edge which clocks a low level on N2-2 to negate BUSY. Negation of BUSY causes U1-8 on board 2 to flag the RDY state for the controller.

If RUN is dropped part way through a sector, the remainder

of the UNIBUS sector is filled with zeros. This is accomplished by ZERO FILL (L) on L2-12 clearing the Drive I/P Buffer for the remainder of the sector.

During the write operation, correctly phased returned write clocks (RET WR CLK) must be sent to the drive along with the write data. This is achieved by delaying R/W CLK through a selectable chain of inverters, D6 and E6. Details for selecting these taps and associated setups for CRC generation etc. (which are factory preset) are given in the Appendix.

the drive sector, by the CRC word. PARITY GATE is turned on by B255 and this allows the CRC checker B5 to validate the CRC word.

GO is reset by 257 EOW PLS and if RUN has previously been cleared by VTDWC, BUSY will be cleared also.

Figure 11 shows the sequence of events for a read operation.

The complete read transfer finally finishes when VTWC overflows and resets I/O GO. This stops the DMA cycles and provides RDY at U1-8 to signify that the controller is able to accept a further command.

6.4.5 WRITE CHECK OPERATION

This function may be performed immediately after writing data to the drive, in order to verify that the data has been correctly stored.

The operation consists of transferring from the UNIBUS to the controller, the same data as has just been written, and comparing it in the controller with the data read back from drive.

The data flow for a write check is as shown by the black arrows on LI-0142 up to the block, on board 4, marked WRITE CHECK.

The data read from the drive is via the white arrows up to the same block.

BD2 A write check operation, functions just as for a write operation as far as board 2 is concerned, except that the line WRCHK (J5-10) is activated.

Write DMA cycles are carried out and an initial seek is performed as for other transfers.

BD4 Board 4 operates partially for a write transfer and partially for a read transfer.

Data from the UNIBUS is converted to bit serial in the SER/DES and compared with SERIAL RD DATA in the same element J2 as is used for the header check. In this instance, since DATA FLD and WR CHK are active on A4-2 and A4-13 respectively, data comparison errors will be clocked at B4-3 to produce WR CHK ERROR.

The clocking signal is derived from R/W CLK and is masked out during PARITY GATE.

The CRC word is normally checked during this operation but if a WR CHK ERR occurs, this will abort the transfer and prevent the CRC being carried out.

6.5. INTERRUPT OPERATION

The controller will generate interrupts to the UNIBUS on error detection and transfer completion if bit 6 is set in VTCS (IDE) and on completion of an actuator movement if bit 13 (AIE) is set.

BD3

The logic on board 3, which initiates an interrupt on RDY (or error detection) is duplicated to interrupt on actuator movement completion. Only the case of RDY interrupts is therefore explained below.

With IDE set, RDY on V5-4 will cause BR to be issued via element outputs V5-6, Y1-6, Y3-3, U3-11 and S5-10. The actual priority level of the bus request is patched on T5 and is pre-wired to BR5.

When BG5 is returned from the arbitrator, it is routed through the grant pass logic for the attention interrupt logic (since this is not requesting an interrupt) to Y1-11.

This delivers a clock edge to V3-11 and since the reset is removed from V3-13 via W3-8, V3-8 switches low to cause SACK to be sent to the UNIBUS.

X1-6 will be high at this time such that, when BBSY is released by the current Bus Master, X2-4 will raise a clock edge on X1-11 to switch X1-8 low. This effectively constitutes BR MSTR at Y3-8 which asserts BBSY to claim ownership of the UNIBUS.

When the previous bus SSYN is finished, Y2-13 clocks X1-3 and causes a low level at V1-12. This 'ands' with V1-11 to generate INTR via X4-6.

BRMSTR, via T3-6, gates out the vector address (patch wired on S2 to 254) through the tristate bus to the bus data line drivers. The sector address is received by the processor when INTR is transmitted, and the processor responds with SSYN which, via V1-8 resets X1 to terminate the interrupt and relinquish use of the UNIBUS.

No further interrupts can occur through this channel until either IDE or RDY are first switched to reset the interrupt logic flip flops to their initial state.

6.6. ERROR CONDITIONS

All error conditions which may arise in the course of an operation are stored in latches in various parts of the controller and cause bit 15 (ERR STAT) to be set in VTCS.

Any error condition will cause the operation to aborted except under certain circumstances explained elsewhere.

The possible error conditions reported through VTDS and VTER are explained below in the order in which they appear in the two registers. All these error status bits are gated on to the tristate bus via 74LS367 bus drivers by STATUS OUT or ERRS OUT.

VTDS (DEVICE STATUS REGISTER)

Bit 12 - HEADER ERROR

This is detected on board 4 as either a sector or track header miscompare and both lines are taken to board 1 where they are combined to give the general condition Header Error (B6-6). In addition the separate conditions are visible through the Maintenance Register VTMNT) in bit position 13 and 14.

A header error may only be considered genuine if the header CRC is valid at the end of the header field, since if not, the apparent header error may be due to a failure to read it correctly from the disc.

Bit 11 - ACTUATOR ADDRESS ERROR

This condition is relayed, on board 1, directly from the drive status indicators and reflects a positioning or timeout error associated with the actuator. A restore operation is needed before this error can be cleared.

This error also causes CHECK to be set.

Bit 9 - CHECK (Unit Unsafe)

CHECK is set for any internal error within the 5017-3. As for Bit 11, it is relayed directly from the drive status lines.

VTER (ERROR REGISTER)

Bit 15 - WRITE PROTECT ERROR

Board 4 detects if the WP bit was set in the header just

checked, and sets this error flag if a write operation is attempted at the current sector address.

Any attempted write operation, header or data,will set the flag if the drive front panel switch is set for the selected disc.

The two conditions are detected through F5-1 and F5-2 respectively.

Bit 14 - UNSAFE ERROR

D3-9 on board 1 sets low to indicate this condition when DRDY (Drive Ready) or ONTRK disappear while GO is active (J2-12), or if a CHECK is detected any time BUSY is asserted at K5-12. In addition, if the drive fails to select when I/O GO is asserted on board 2, D3-11 will be clocked to transfer a low level from C5-6 to D3-9.

Bit 13 - BAD SECTOR DETECTED

If the bad sector bit is set in the current sector header, board 4 sets C1-9 active low. This is clocked through to B1-5 if a transfer to this sector is attempted, when DFP is generated at the start of the data field. B1-5 indicates the condition BAD SECT VIOLN.

Bit 12 - NON EXISTENT TRACK

Track address values up to 7777 can be loaded into VTTA but values above 4017 are non existent addresses which are detected on board 1 by logic elements K3, H3, J3 and D5 to generate NON EXIST TRK.

If a transfer is attempted with NON EXIST TRK active, A1-3 on board 4 will be clocked, when BUSY is asserted, to generate this error condition.

Bit 11 - NON EXISTENT SECTOR

Values up to 77 can be loaded into VTSA but values above 30 are non-existent addresses.

The contents of VTSA are monitored on board 1 by comparators H4 and J4 which produce NON EXIST SECT at J4-7 for values 31 through 77.

Board 4 uses NON EXIST SECT to set A1-9 high (ILL SECT VIOLN) when BUSY is asserted.

Bit 10 - PROGRAMME ERROR

This is set on board 2 by any one of three conditions as follows:-

If VTWC has not been loaded before commencing a transfer, Y1-6 will remain high. A request to perform any transfer will be recognised by a high level on W1-11 so that when GO DLY(L) is active on N2-6, W1-8 will produce a low level which, via W2-10, clears Y2 to flag PROG ERR.

The same level change from W1-8 clocks Y2-3 so that, if the drive has failed to select, and Y2-2 is low, Y2-5 will switch low to give the error condition.

The third condition is that if the controller is already active with a transfer, as indicated by a low level on N2-9, when an attempt is made to initiate a new transfer, N2-8 switching low will provide an alternative path for setting the error flip flop.

Bit 9 -- HEADER CRC ERROR

This is detected on board 4 by flip flop C3 as explained in section 6.4.2.2.

Bit 7 - BATA CRC ERROR

This is detected by flip flop B4 on board 4 and operates in the same way as for the header CRC.except that A3-8 directs the clock edge to B4-11 during the data field.

Bit 4 - TRANSFER ERROR

Once serial data is flowing to or from the disc drive,it is essential to process the data without break (since the disc cannot be stopped!)

Logic linked to the SER/DES on board 4 checks that this rule is not broken during both write and read operations.

If during a write operation, L5-5 is still high when J4-5 fires, indicating a fresh I/P Buffer loading pulse, DATA IN LATE (L) is directed to P1-4 to set the condition XFER ERR.

During a read operation, if L2-9 shows that the Drive O/P Buffer still has a word of data when L2-10 goes high, indicating an O/P Buffer load pulse, then P1-3 will set

the error condition.

Bit 3 - WRITE CHECK ERROR

This is covered by section 6.4.5.

Bit 2 - NON EXISTENT MEMORY

This error condition is set by failure of the UNIBUS to respond with SSYN within approx. 20 µS of the 8401-3 attempting a DMA. Section 6.4.1.1. explains the logic involved.

Bit 1 - END OF PACK

D4-12 on board 1 detects selection of the last track on the selected disc and if a track increment pulse clocks F5-3 in this condition, F5-5 will flag PLATT OVFL status which reports End of Pack to the UNIBUS.

7.0 FAULT FINDING

If problems arise with the 8401-3 system during operational use, the test software supplied with the equipment should be run in order to identify the type of fault.

Once a fault is located, the debug programme VTDBG may assist in finding the cause of the fault by enabling repetitive transfers to be performed as specified by operator intervention via the keyboard.

The software provided, is described in the Appendix.

The DEC software utility "ODT" is very useful for fault finding since it aids the writing of simple routines for performing basic data transfers or seek operations.

An example is given below of the most basic programme required to perform a repetitive transfer.

Address	Contents	Operation
1000	12706	sets stack pointer
1002	1000	
1004	12737	
1006	00XXXX	loads VTTA
1010	176722	
1012	12737	
1014	0000YY	loads VTSA
1016	176724	
1020	12737	
etc	ZZZZZZ	loads VTBA
	176720	
	12737	loads 2's complement
	177400	of 256 words into
	176716	VTWC
	12737	
	FFFF	loads disc and func-
	176714	tion into VTCS
	105737	
	176714	loops, waiting for
	100375	ready status
	137	jumps back to
1052	1000	start of programme

Fig. Basic Program

Address 1000 is used as the start address simply because this is the lowest address where a programme may normally be expected to reside.

The routine starts by loading the stack pointer. This is always good practice as it gives protection in the event of unexpected processor 'traps'.

XXXX and YY will normally be any legal track and sector addresses respectively.

ZZZZZZ will be any UNIBUS address well outside the programme area to allow for alterations to the programme.

FFFF specifies unit, disc and function bits relevant to the transfer.

The last instruction jumps to the start of the programme so that the transfer will repeat indefinitely. If the destination of the jump (location 1052) is changed from 1000 to 1020, then each transfer will start at the next sector address until the end of the disc is reached.

If the programme is loaded with the use of "ODT", then breakpoints may be set where required, to examine device register contents immediately after a transfer has completed or to examine the buffer area after a read operation.

When using an oscilloscope to trace controller problems, if the fault appears to be related to signal transfer between the drive and controller, it must be realised that signal levels in the differential cables, can be as low as 25mV and as such, care must be taken in ascertaining whether a signal is active or not.

FIG 1 8401_3 Board Positions

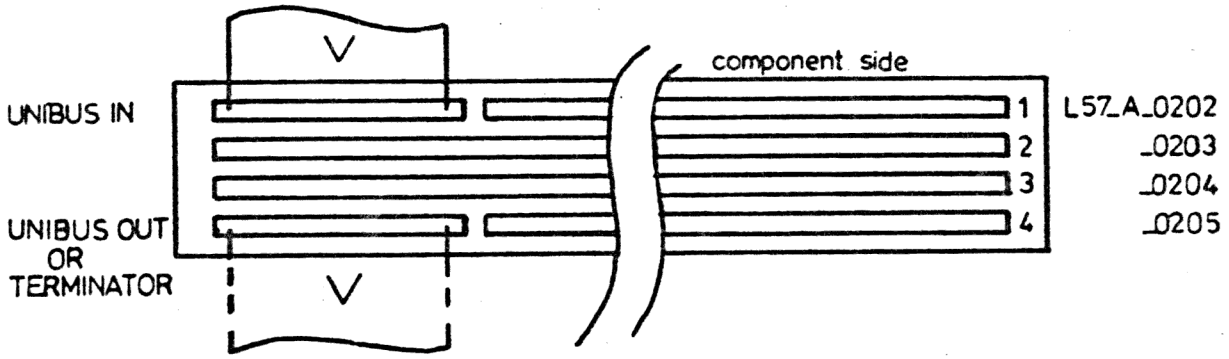


FIG 2 Drive Cabling Arrangements

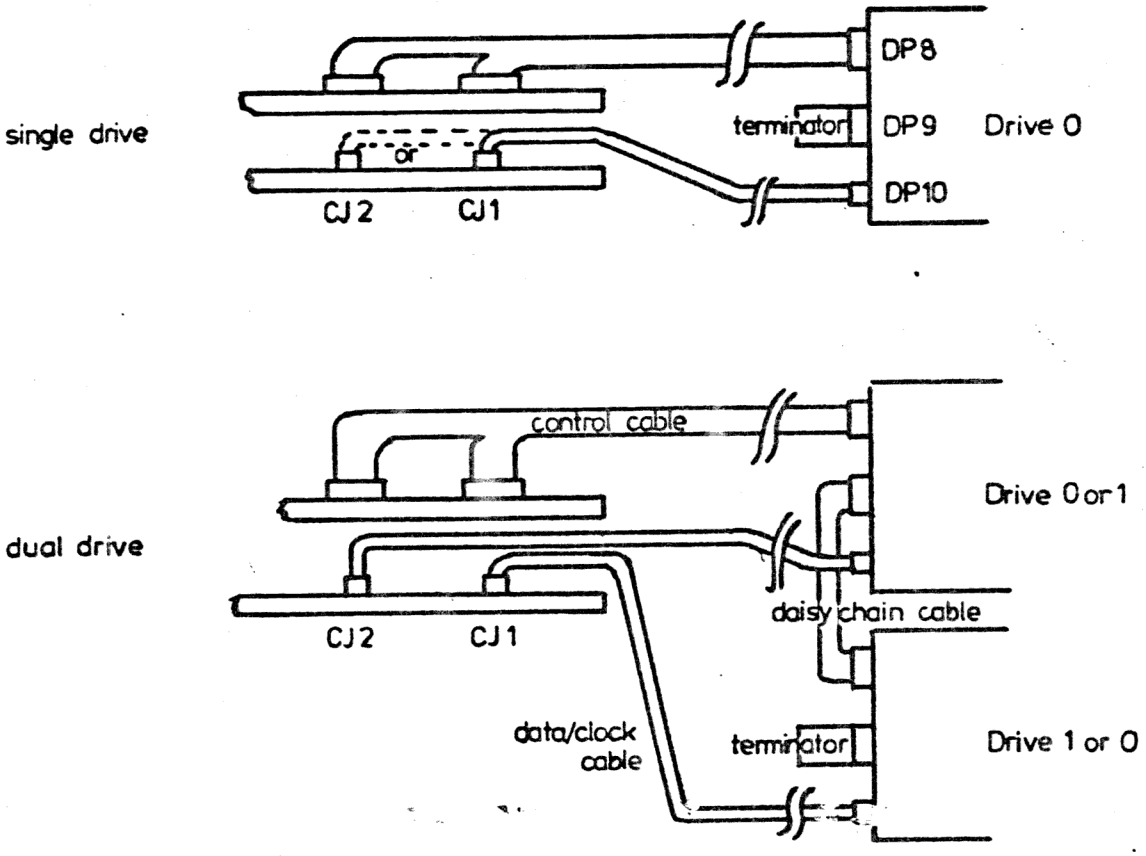


FIG 3 Drive/UNIBUS Sectors at Index

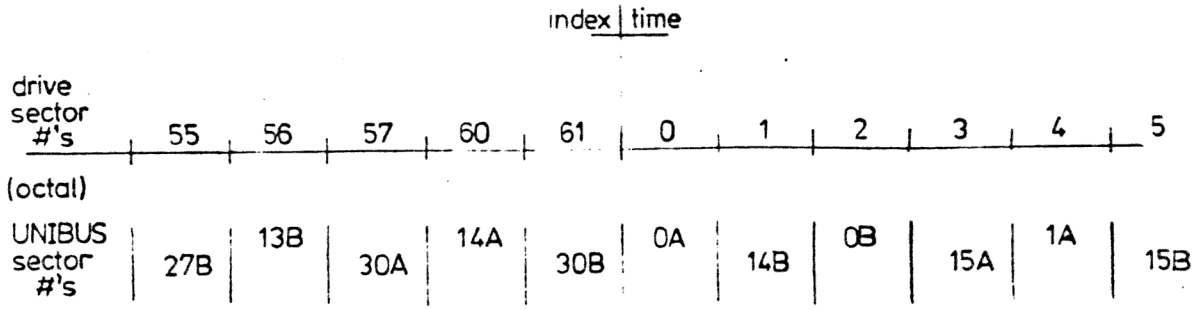


FIG 4 Drive Sector Format

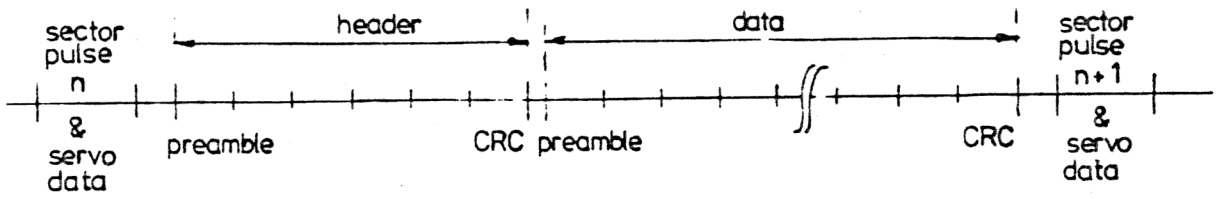


FIG 5 Device Address Structure

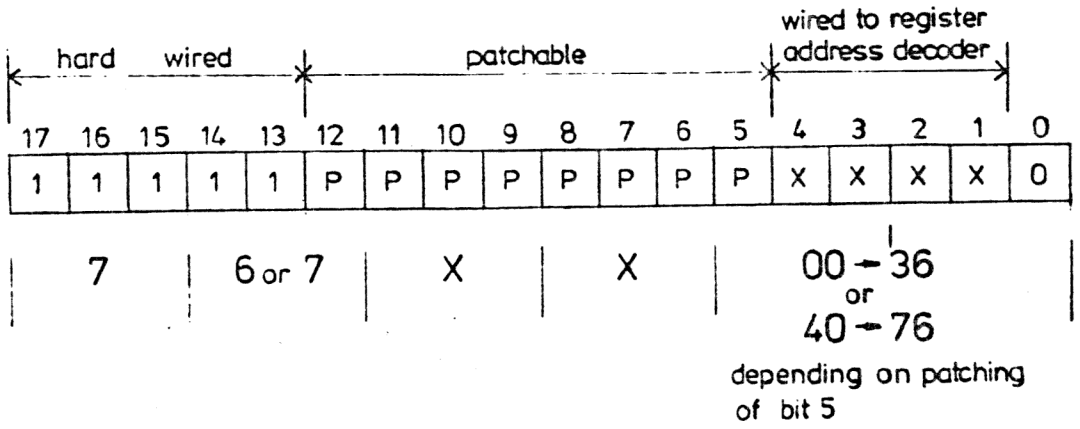


FIG 6 Block Diagram Register Schematic

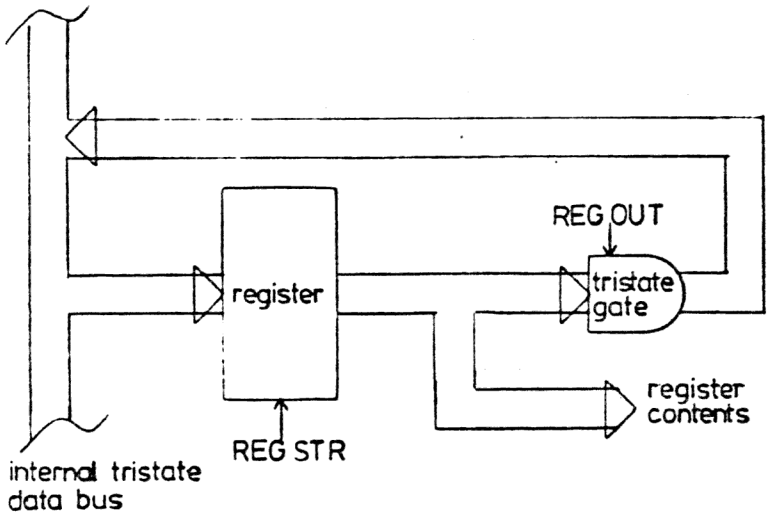


FIG 7 Register Loading & Reading

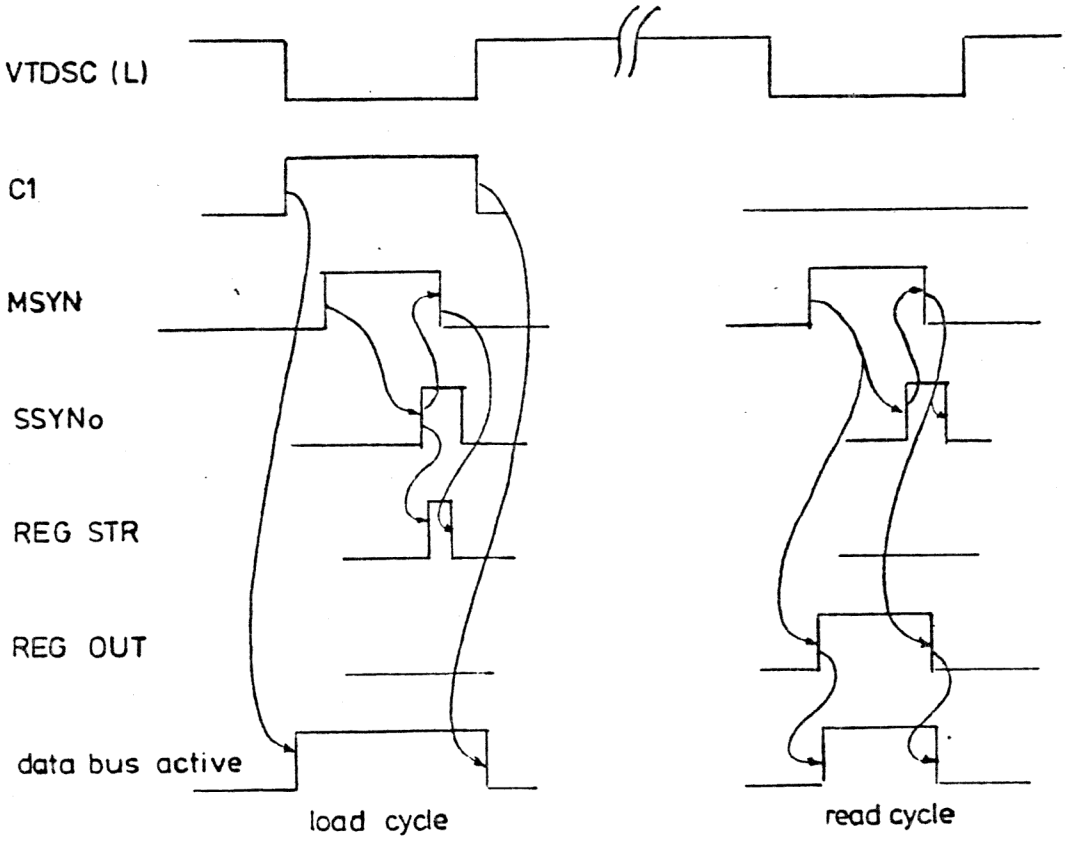


FIG 8 Initiation of Seek Operation

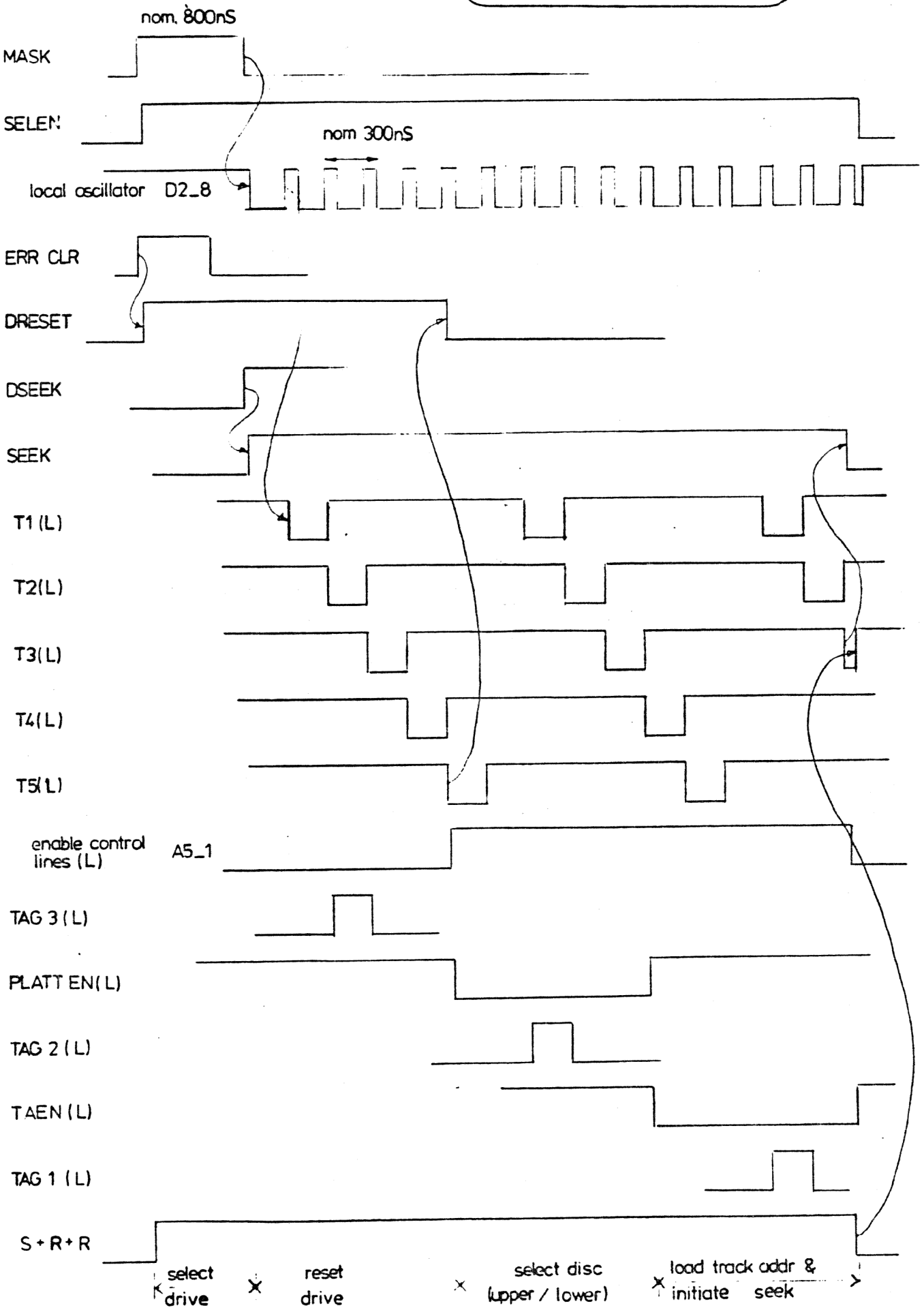
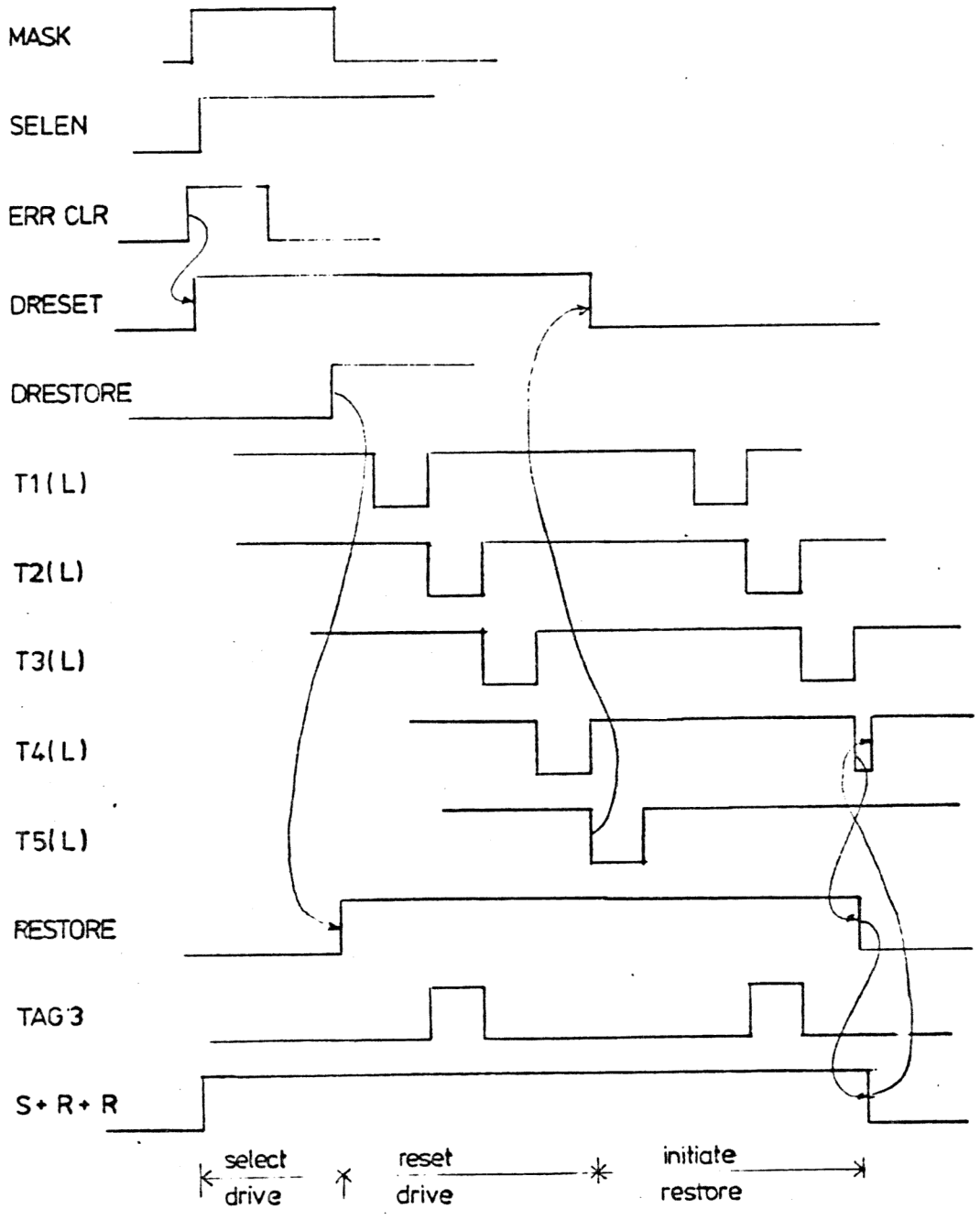


FIG 9 Initiation of Restore Operation



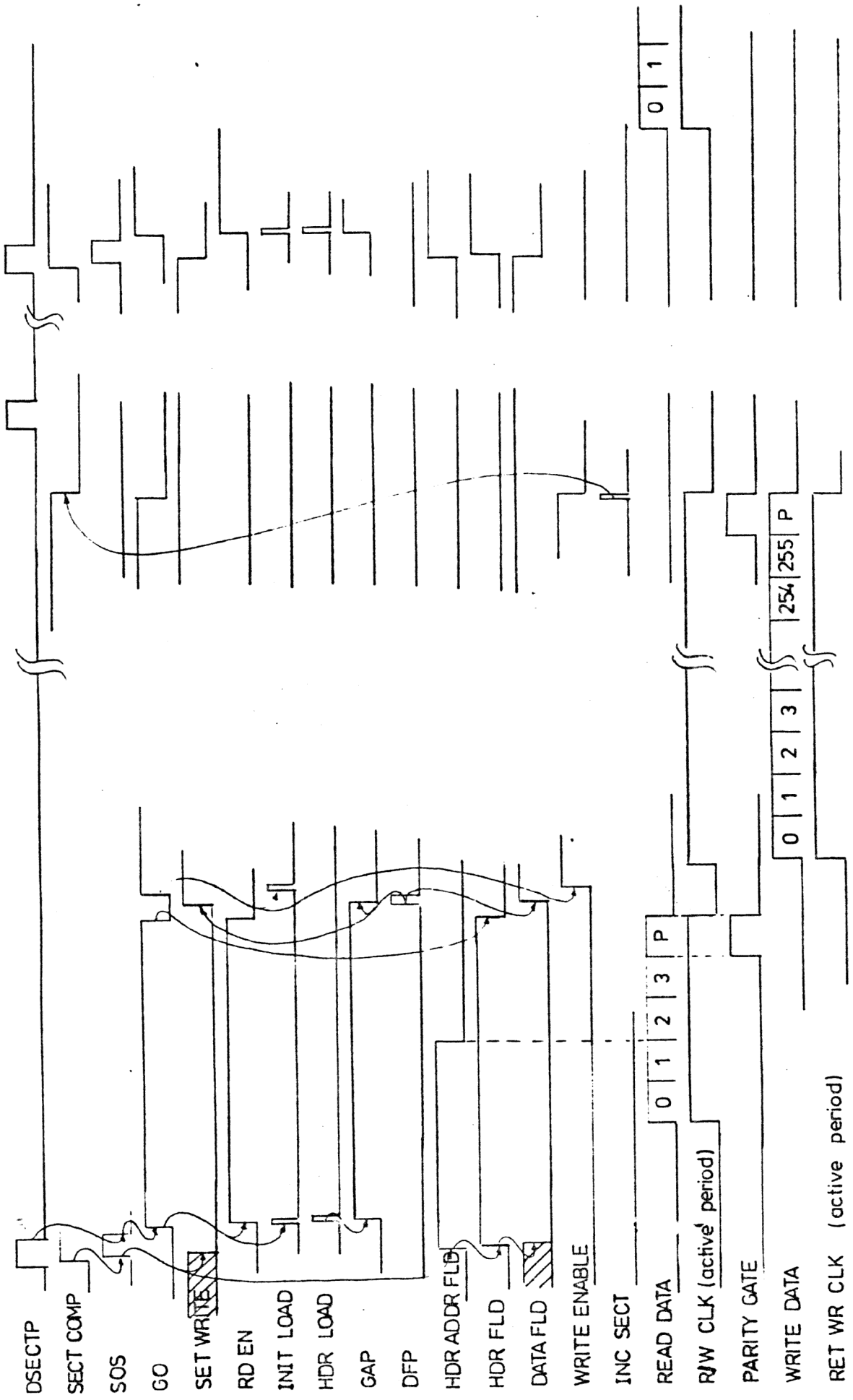


FIG 10 WRITE OPERATION

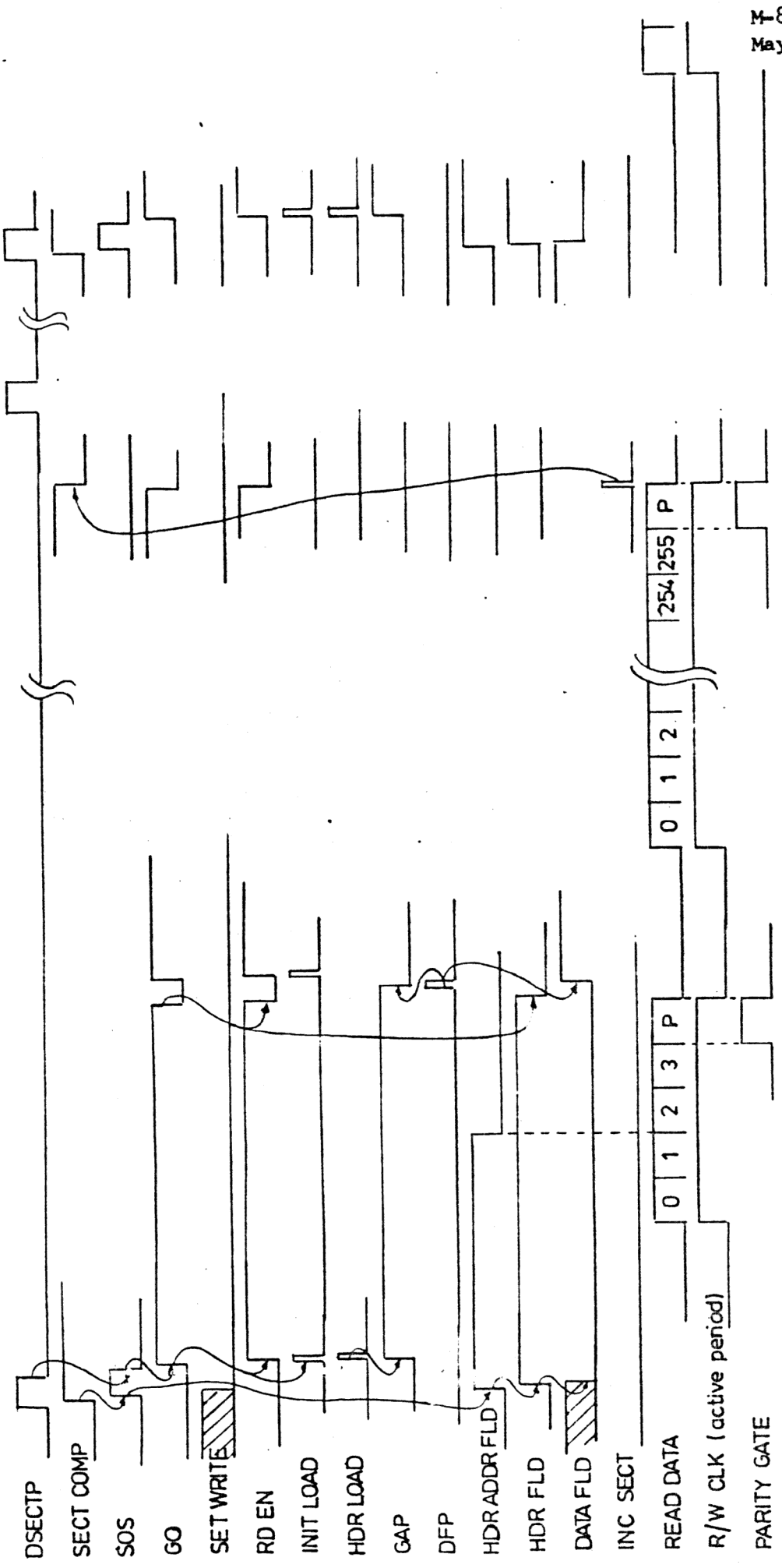


FIG 11 READ OPERATION

APPENDIX

A. LOGIC DIAGRAM CONVENTIONS

The controller boards used in the 8401-3 carry integrated circuit packages arranged in a row and column matrix. A particular I.C. position is identified by a row number and a column letter. This identification appears in the logic diagrams as a letter/number pair normally enclosed within each logic element. Under the positional reference is marked the last two or three digits of the I.C. type. The majority of I.C.s are 74LS types, so that a 74LS166 shift register, for example, is shown as block with 166 marked under the position reference.

In cases where Schottky logic is used, the I.C type reference in the logic diagrams is preceded by the letter "S".

B. RELATED SOFTWARE

The software associated with the 8401-3 is available on floppy disc or papertape, and consists of static and dynamic tests, a 'debug' programme and a header utility.

Details of these programmes are provided in the relevant programme listings, the front sheets of which are appended to this section of the Appendix.

RT-11 PROGRAM RUNNING FROM FLOPPY DISC. (REV A)

TO ACTIVATE THE RT-11 SYSTEM MONITOR, PERFORM THE FOLLOWING OPERATIONS:-

1. LOAD THE RELEVANT FLOPPY DISC INTO THE DRIVE.
2. PRESS THE COMPUTER SWITCH "BOOT/INIT" (OR USE THE CPU SWITCHES TO BOOT THE FLOPPY DIRECTLY AND SKIP STEP 3.)- THE TELETYPE WILL PRINT FOUR 6 DIGIT NUMBERS FOLLOWED BY A "$" SIGN.
3. TYPE "DX" FOLLOWED BY "RETURN" (SUBSEQUENTLY REFERRED TO AS <CR>)
4. THE RT-11 OPERATING SYSTEM WILL BE READ FROM THE FLOPPY DISC AND A DOT WILL BE PRINTED BY THE TELETYPE INDICATING THAT THE MONITOR IS READY TO ACCEPT A COMMAND.

N.B. ALL COMMANDS TO THE MONITOR CONSIST OF AN INSTRUCTION, FOLLOWED BY A SPACE, FOLLOWED BY A FILENAME OR AN ADDRESS (SEE EXAMPLES LATER).

THE PROGRAMS ASSOCIATED WITH THE 8401-3 SYSTEM ARE AS FOLLOWS:-

VTHDR.SAV	ENABLES LISTING/MARKING OF BAD SECTORS AND/OR WRITE PROTECTED SECTORS ON THE 5017-3 DRIVE. (SUPERCEDES "MKRLST.SAV")
VTRANP.SAV	PERFORMS A RANDOM ADDRESS & DATA TEST.
VTLTFP.SAV	PERFORMS A RANDOM DATA, INCREMENTING ADDRESS TEST.
VTDBG.SAV	A COMPREHENSIVE DEBUGGING AID ENABLING VARIOUS TRANSFER TYPES TO BE RUN ON ALL OR PART OF THE DISC. THE TRANSFER PARAMETERS ARE READILY MODIFIED FROM THE TERMINAL KEYBOARD.
VTST.SAV	PERFORMS TESTS ON THE SUBSYSTEM TO CHECK THE BASIC OPERATION OF THE CONTROLLER. MAY BE RUN IN PART WITHOUT A DRIVE CONNECTED.
VTCERT.SAV	A THREE PART TEST TO SUPERCEDE VTRANP & VTLTFP. PROVIDES OPERATION UNDER INTERRUPTS, 1 OR 2 DRIVE TESTING, BAD SECTOR LISTING, INCREMENTING ADDRESS MODE AND RANDOM MODE (DATA, BLOCK LENGTH, ADDRESS, & PLATTER SELECT). (AVAILABLE, BUT STILL UNDER DEVELOPMENT)

TO RUN ANY OF THE ABOVE PROGRAMS, TYPE "R FILENAME".
E.G. TO RUN VTDBG.SAV, TYPE "R VTDBG" (NOTE THAT IT IS NOT NECESSARY TO TYPE ".SAV")

AFTER STARTING A PROGRAM RUNNING, THE FLOPPY DISC SHOULD BE RELEASED FROM THE DRIVE IF IT IS NOT LIKELY TO BE USED FOR A WHILE.

IF IT IS DESIRED TO ALTER PROGRAM CONSTANTS PERMANENTLY, USE "PATCH" AS FOLLOWS:-

TYPE "R PATCH" ; THEN SPECIFY THE FILE NAME AS REQUESTED.
AFTER "*" IS PRINTED,PATCH RUNS MUCH LIKE ODT ALLOWING THE SAME USE OF "/",CR, LF, AND "^".
WHEN PATCHING IS COMPLETE, TYPE "E" TO RETURN TO THE MONITOR, OR "F" TO PATCH ANOTHER FILE.

```
;TITLE: 8401-3 HEADER UTILITY PROGRAM

;PART NUMBER:   -SOURCE: CB4-1-DDA-B7-11-A
;               -BINARY: CB4-1-DDB-B7-11-A

;WRITTEN:       DEC 79
;LAST MODIFIED: 8/1/80

        .TITLE VTHDR-HEADER UTILITY PROGRAM
        .MCALL ..V2...REGDEF,.EXIT
        ..V2..
        .REGDEF
        .ASECT
        .NLIST TTM
        .ENABL LC

PS=177776

; The HEADER UTILITY PROGRAM provides the 8401-3 user with
; the following maintenance facilities relating to the disc sector headers:-

;       1. FORMAT - This writes the mandatory sector headers on the lower and/or
;                   upper disc. It will normally be used for virgin media only.

;       2. MARK - This mode enables individual headers to be marked "BAD" or "PROTECTED"
;                   as specified in the opening dialogue.
;                   "BAD" indicates that the sector has been found to be unreliable
;                   with regard to data storage or recovery and needs to be ignored
;                   in subsequent data transfers. It effectively makes 'soft' errors
;                   become permanently 'hard' and the software has to deal with them
;                   accordingly.
;                   "PROTECTED" means that the sector so marked is protected from
;                   being corrupted by future write operations.
;                   Headers previously marked can be 'un-marked' by using the
;                   'CLEAR' sub-mode.

;       3. LIST - This causes the specified disc/s to be read to determine the
;                   status of all the headers. The address of "BAD" or "PROTECTED"
;                   sectors is printed along with the totals of each.

;       4. READ - The four header words of any specified sector maybe printed out to
;                   inspect their contents. Several consecutive headers may be listed
;                   by specifying the number as the last figure in the input.


;       At any time:-   CTRL C - Returns control to the RT-11 monitor.
;                       CTRL R - Restarts at the opening dialogue.
;                       CTRL H - Performs a RESTORE to track zero.
;       and during the 'MARK' mode:-
;                       CTRL L - Switches to the lower disc.
;                       CTRL U - Switches to the upper disc.

.=40
.+ORD 200,1000
```

```
;TITLE:          8401-3 DEBUG PROGRAM

;PART NUMBER:    -SOURCE: L84-1-DDA-63-11-C1
;                -BINARY: L84-1-DDB-63-11-C1

;WRITTEN:        29/9/77

;LAST MODIFIED:  21/1/80


;1.0 SYSTEM REQUIREMENTS

;       PDP11 SERIES COMPUTER (MIN 8K CORE)
;       8401-3 DISC DRIVE SYSTEM
;       I/O TERMINAL
;       PAPERTAPE READER OR
;       FLOPPY DISC DRIVE



;2.0 PRE-REQUISITES

;AREAS TO BE WRITTEN ON THE DISC, MUST FIRST HAVE THE
;HEADER FIELD WRITTEN WITH THE CORRECT HEADER ADDRESS.
;THIS CAN BE ACHIEVED EITHER BY FORMATTING THOSE
;AREAS WITH A WRITE HEADER OP. USING THIS PROGRAM,
;OR BY FORMATTING THE WHOLE DISC SURFACE USING THE
;"HEADER UTILITY PROGRAM" (VTHDR). PART NO. L84-1-DDB-67-11


;3.0 OPERATING INSTRUCTIONS

;AFTER LOADING, START THE PROGRAM AT 200.
;AFTER TYPING "A"OR "D" IN RESPONSE TO THE FIRST
;QUESTION, THE PROGRAM WILL ASK FOR PARAMETERS
;TO BE DEFINED, ACCORDING TO WHICH TESTS ARE TO BE
;PERFORMED, AS FOLLOWS:-   (IN ALL CASES, TYPE A
;"RETURN [CR]" AFTER THE ANSWER)
```

```
;DATA TESTS.

;REQUEST          RESPONSE                    EFFECT

;"(O)PTIONS"      100000   INHIBITS ADDR.  INC ON ERR.
;                  40000   INHIBITS BELL ON ERROR-THE
;                          BELL IS AUTOMATICALLY
;                          INVOKED IF ERROR PRINTING
;                          IS INHIBITED UNLESS THIS BIT
;                          IS SET.
;                  20000   INHIBITS DATA COMPARE
;                          ERROR PRINTOUTS.
;                  10000   INHIBITS STATUS ERROR PRINTOUTS.
;                   4000   CAUSES THE PROGRAM TO HALT
;                          AFTER A DATA COMPARE ERROR.
;                   2000   CAUSES A HALT AFTER A STATUS
;                          ERROR
;                   1000   SELECTS UNIT #1
;                    400   SELECTS THE REMOVABLE DISC
;                    200   ENABLES THE ADDR.  TO BE
;                          INCREMENTED BY THE AMOUNT
;                          DEFINED IN "(A)DDR.  (I)NC"
;                    100   ENABLES OPERATION WITH INTERRUPT.
;                     40   NOT USED
;                     20   WILL COMPARE DATA READ
;                          FROM DISC WITH THAT IN WRITE
;                          BUFFER.
;                     10   SPECIFIES A HEADER OPERATION.
;                      4   SPECIFIES A WRITE CHECK FUNCTION.
;                      2   DITTO - READ OPERATION.
;                      1   DITTO - WRITE OPERATION.

;"(S)ECTOR"       0 - 30   SPECIFIES A VALID STARTING
;                          SECTOR ADDRESS.
;                 >30      IS ALLOWED BUT WILL CAUSE A
;                          NON EXISTENT ADDR.  ERROR.
;                 >77      DIGITS >77 WILL BE IGNORED.

;"(T)RACK"        0-4017   SPECIFIES A VALID STARTING
;                          TRACK ADDRESS.
;                 >4017    IS ALLOWED BUT WILL CAUSE A
;                          NON EXISTENT ADDR.  ERROR.
;                 >7777    DIGITS >7777 WILL BE IGNORED.

;"(A)DDR.  (I)NC"          NNNNNN  SPECIFIES AMOUNT BY WHICH
;                          SECTOR ADDR.  IS INCREMENTED
;                          BEFORE EACH NEW TRANSFER CYCLE.
;                          N. B.  200 MUST BE SET IN "OPTIONS"
;                          TO ENABLE ADDRESS INCREMENT.

;"(W)D.  (C)NT"   1-6000   WILL BE THE TRUE LENGTH IN
;                          WORDS OF EACH TRANSFER.  THE
;                          PROGRAM CONVERTS THIS INTO
;                          TWO'S COMPLEMENT.  ALSO, ON
;                          APPROACHING THE END OF THE DISC,
;                          THE PROGRAM MODIFIES THE TRANSFER
;                          LENGTH TO PREVENT PACK OVERFLOW.
;                          ON RETURNING TO THE BEGINNING OF
;                          THE DISC, THE SPECIFIED WORD COUNT
;                          IS RESUMED.
;                          THE FINISHING VALUE OF VTBA
;                          IS CALCULATED AND CHECKED AFTER
;                          EVERY TRANSFER.
```

;"(D)ATA"	NNNNNN	THE DATA TO BE USED FOR WRITE AND WRITE CHECK OPERATIONS; AND AS THE DATA REFERENCE IN DATA COMPARE OPERATIONS.
;"(D)ATA (I)NC."	N 4	CAUSES THE DATA TO BE INCREMENTED EACH XFER CYCLE.
	2	CAUSES THE TRACK & SECTOR ADDRESS TO BE USED AS DATA. (THIS OPTION WILL CAUSE THE CONTENTS OF "DATA" TO BE IGNORED).
	1	CAUSES DATA INCREMENT BY WORD.

;ACTUATOR TESTS.

;REQUEST	RESPONSE	EFFECT
;"(O)PTIONS"	100000	WILL INHIBIT TRACK ADDR. CHANGE AFTER DETECTION OF AN ERR.
	40000	INHIBITS THE BELL ON ERROR. THE BELL IS RUNG ON ERR. DET'N IF REGISTER PRINTOUT IS INHIBITED UNLESS THIS BIT IS SET.
	20000	EN. ATTN. INT. HANDLING
	10000	INHIBITS PRINTING OF REGISTER CONTENTS ON DET'N OF AN ERROR.
	4000	NOT USED.
	2000	STOPS THE PROGRAM ON ERR. DET'N.
	1000	SELECTS UNIT #1.
	400	SELECTS THE REMOVABLE DISC.
	200	NOT USED
	100	ENABLES OPERATION WITH "DONE" OR "ERROR" INTERRUPT.
	40	NOT USED.
	20	NOT USED.
	10	NOT USED.
	4	ENABLES A HEADER CHECK TO BE PERFORMED.
	2	A RESTORE WILL BE PERFORMED AFTER EVERY SEEK.
	1	THE HEADS WILL MOVE BETWEEN THE TWO ADDRESSES SPECIFIED
;"TRK 1" (T1)	0-4017	DEFINES THE BASE ADDR.
	>4017	NOT ACCEPTED-THE REQUEST WILL BE MADE AGAIN.
;"TRK 2" (T2)	0-4017	DEFINES THE 2ND ADDR.
	>4017	NOT ACCEPTED-AS TRK 1.
;"(A)DDR. (I)NC"	0-4017	DEFINES AMOUNT BY WHICH TRK 2 IS UPDATED AFTER EACH ACCESS.
;"(R)ATE"	NNNNNN	CAUSES A WAIT TO BE INSERTED BETWEEN EACH SEEK. THE TIME BEING DEPENDENT ON "N" AND THE PROCESSOR TYPE.

```
;ONCE A PARTICULAR OPERATION IS IN PROGRESS, A REVISED
;OPERATION CAN BE DEFINED BY TTY CONTROL INPUTS AS
;FOLLOWS:-

;CTRL R CAUSES THE PROGRAM TO RESTART WITH THE OPENING
;       DIALOGUE.

;CTRL A ENABLES THE OPERATOR TO ALTER ANY OF THE
;       OPERATION PARAMETERS THUS:-
;       THE TTY WILL PRINT "PARAMETER?" AND THEN
;       PRINT THE PROMPTING CHARACTER "*".
;       TYPE IN THE INITIAL LETTER OF THE PARAMETER AS
;       PER THE ORIGINAL REQUESTS, FOLLOWED BY A CR.
;       THE ORIGINAL VALUE WILL BE PRINTED AFTER WHICH
;       THE NEW VALUE SHOULD BE TYPED FOLLOWED
;       BY A CR.  TYPING A CR ALONE WILL CAUSE THE
;       ORIGINAL VALUE TO REMAIN UNALTERED.

;       TYPING "G" [CR] WILL RESUME THE SELECTED
;        OPERATION.

;CTRL C RETURNS CONTROL TO THE MONITOR.


;CTRL O WILL START ODT.  THE START ADDRESS OF ODT
;       IS LOCATED AT LOCN.  "ODT".  IT IS CURRENTLY
;       40172.
;       N.B.  ODT MUST HAVE BEEN LOADED
;       PRIOR TO "VTDBG" BY TYPING  GE ODT".
```

```
;TITLE:          8401-3 LONG TERM TEST
;       (PRINT ALL ERRORS)

;PART NUMBER:    -SOURCE: L84-1-DDA-65-11-E1
;                -BINARY: L84-1-DDB-65-11-E1

;WRITTEN:        15/3/78

;LAST MODIFIED: 8/1/80
;       (PART NUMBER ALTERED FROM "-61-" TO "-65-" )


;SYSTEM REQUIREMENTS

;       PDP11 SERIES COMPUTER (MIN 8K CORE)
;       8401-3 DISC DRIVE SYSTEM*
;       I/O TERMINAL
;       PAPERTAPE READER

;       *SET TO UNIT 0


;2.0 OPERATING INSTRUCTIONS

;THE PROGRAM STARTS AT ADDRESS 200.
;AFTER STARTING, CERTAIN QUESTIONS ARE ASKED TO
;ESTABLISH TEST CONDITIONS.
;  TYPE A SINGLE LETTER ANSWER FOLLOWED BY A
;"CR" IN ALL CASES.
;ONCE THE TEST IS RUNNING, TYPING A "C" IN
;CONJUNCTION WITH THE "CTRL" KEY WILL CAUSE
;A RETURN TO THE MONITOR.

;TYPING "CTRL R" WILL CAUSE THE PROGRAM TO RESTART.



;3.0 TEST DEFINITIONS

;THE PROGRAM FILLS THE WRITE BUFFER WITH RANDOM
;DATA AND WRITES THIS TO THE DRIVE, STARTING
;AT A RANDOMLY SELECTED ADDRESS ON THE DISC SPECIFIED
;BY THE OPERATOR.  DATA IS TRANSFERRED IN 12 SECTOR BLOCKS.
;THE TRANSFER STATUS IS CHECKED AFTER EACH WRITE
;OPERATION AND ERRORS REPORTED ON THE I/O TERMINAL.
;THE SAME BLOCK IS THEN READ BACK, CHECKED FOR
;CORRECT STATUS, AND COMPARED WITH THE DATA WRITTEN.
;THE FIRST COMPARE ERROR DETECTED WILL TERMINATE
;THE COMPARE ROUTINE AND A NEW WRITE TRANSFER WILL
;BE COMMENCED.
;STATUS AND COMPARE ERRORS ARE REPORTED AS DETAILED
;IN SECTION 4.0
;THE PROCESS IS THEN REPEATED UNTIL THE SELECTED
;DISC HAS COMPLETED AN ARBITRARY NUMBER OF TRANSFERS, AND
;THEN CONTINUED ON THE OTHER DISC IF SO SPECIFIED.
;TRANSFERS ARE ATTEMPTED UP TO THREE TIMES FOR STATUS
;ERRORS BEFORE PROCEEDING TO A NEW ADDRESS.  THE
;LOCATIONS "WRTRY" AND "RDTRY" MAY BE PATCHED FOR
;ANY NUMBER OF TRANSFER ATTEMPTS.  DATA COMPARE ERRORS
;ARE REPORTED IMMEDIATELY ON DETECTION.
;SECTORS WHICH REPEATEDLY SHOW ERRORS, MAY BE
;MARKED "BAD" ( AND SUBSEQUENTLY IGNORED )BY RUNNING
;THE PROGRAM AFTER TYPING "Y" TO THE APPROPRIATE OPENING QUESTION.
;HEADER ERRORS WHICH ARE DETECTED WITHOUT HEADER
;CRC ERRORS AUTOMATICALLY CAUSE A RESTORE TO BE
;PERFORMED.
```

```
;4.0 ERROR REPORTS

;STATUS ERRORS ARE REPORTED BY PRINTING THE CONTENTS
;OF THE MAIN WORKING 8401-3 REGISTERS IN THE FORMAT
;SHOWN BELOW:-

;DS=****** ER=****** CS=****** WC=****** BA=****** TA=****** SA=******

;IF THIS APPEARS AFTER A WRITE TRANSFER, THE ADDRESS
;WILL BE MODIFIED AND A NEW WRITE OPERATION STARTED.
;DATA COMPARISON ERRORS WILL BE REPORTED AS FOLLOWS:-

;DATA ERROR AT TRK**** SECT** WORD******

;        DATA WAS ******  SB ******

; AN "R"  AFTER THE REGISTER CONTENTS INDICATES THAT
;A "RESTORE" WAS PERFORMED BEFORE RETRYING THE TRANSFER.
; AN "E" INDICATES THAT THE TRANSFER IS STILL IN ERROR AFTER
;THE MAXIMUM NUMBER OF RETRIES HAVE BEEN ATTEMPTED.

;IF A STATUS ERROR IS DETECTED DURING A READ TRANSFER,
;NO DATA COMPARISON IS MADE, SINCE IT IS PROBABLE
;THAT THE DATA WORD IN QUESTION WILL BE LOST IN THE
;SILO BUFFER WHEN THE ERROR OCCURRED.
;THE MESSAGE "DONE UPPER (OR LOWER)" IS PRINTED ON COMPLETION OF THE
;APPROPRIATE DISC.

;A MAXIMUM ERROR COUNT OF 128 IS ALLOWED AFTER
;WHICH THE PROGRAM AUTOMATICALLY STOPS.
;LOCATION "ERMAX" MAY BE PATCHED TO ALTER THIS.


;5.0 RUN TIME

;THE PROGRAM TAKES APPROX.  20 MINS TO TEST ONE DISC.

        .TITLE VTRANP
        .MCALL ..V2.,.EXIT
        ..V2..
        .ASECT
        .NLIST TTM
        .NLIST SEQ
```

```
;TITLE:          8401-3 LONG TERM TEST (VTLTFP)
;                -PRINTS ALL ERRORS
;        (RANDOM DATA, INCREMENTING ADDRESS)

;PART NUMBER:    -SOURCE: L84-1-DDA-61-11-D1
;                -BINARY: L84-1-DDB-61-11-D1

;WRITTEN:        MAY 1978

;LAST MODIFIED: 12/6/79
;(.TITLE DIRECTIVE CHANGED FROM "VTTEM" TO "VTLTFP" )


;SYSTEM REQUIREMENTS

;       PDP11 SERIES COMPUTER (MIN 8K CORE)
;       8401-3 DISC DRIVE SYSTEM*
;       I/O TERMINAL
;       PAPERTAPE READER OR-
;       FLOPPY DISC DRIVE

;       *SET TO UNIT 0


;2.0 OPERATING INSTRUCTIONS

;THE PROGRAM STARTS AT ADDRESS 200.
;AFTER STARTING, CERTAIN QUESTIONS ARE ASKED TO
;ESTABLISH TEST CONDITIONS.
; TYPE A SNGLE LETTER ANSWER FOLLOWED BY A
;"CR" IN ALL CASES.
;ONCE THE TEST IS RUNNING, TYPING AN "R" IN
;CONJUNCTION WITH THE "CTRL" KEY WILL CAUSE
;THE PROGRAM TO RESTART.
;TYPING  "CTRL C" WILL RETURN CONTROL
;TO THE MONITOR. (INVALID WITH PAPERTAPE SYSTEM)


;3.0 TEST DEFINITIONS

;THE FIRST TWO WORDS OF THE WRITE BUFFER ARE RANDOMLY
;GENERATED AND THEN INCREMENTED TO FILL THE REMAINDER.
;THE PROGRAM THEN WRITES THIS TO THE DRIVE, STARTING
;AT SECTOR 0, TRACK 0 OF THE DISC SPECIFIED
;BY THE OPERATOR.
; DATA IS TRANSFERRED IN 12 SECTOR BLOCKS.
;THE TRANSFER STATUS IS CHECKED AFTER EACH WRITE
;OPERATION AND ERRORS REPORTED ON THE I/O TERMINAL.
;THE SAME BLOCK IS THEN READ BACK, CHECKED FOR
;CORRECT STATUS, AND COMPARED WITH THE DATA WRITTEN.
;THE FIRST COMPARE ERROR DETECTED WILL TERMINATE
;THE COMPARE ROUTINE AND A NEW WRITE TRANSFER WILL
;BE COMMENCED.
;STATUS AND COMPARE ERRORS ARE REPORTED AS DETAILED
;IN SECTION 4.0
;THE PROCESS IS THEN REPEATED UNTIL THE SELECTED
;DISC IS COMPLETED, AND THEN CONTINUED ON THE OTHER
;DISC IF SO SPECIFIED.
;TRANSFERS ARE ATTEMPTED UP TO THREE TIMES FOR STATUS
;ERRORS BEFORE A NEW ADDRESS IS SELECTED  THE
;LOCATIONS "WRTRY" AND "RDTRY" MAY BE PATCHED FOR
;ANY NUMBER OF TRANSFER ATTEMPTS.  DATA COMPARE ERRORS
;ARE REPORTED IMMEDIATELY ON DETECTION AND NOT RETRIED.
;SECTORS WHICH REPEATEDLY SHOW ERRORS, MAY BE
;MARKED "BAD" BY RUNNING THE PROGRAM AFTER TYPING "Y"
```

```
;TO THE APPROPRIATE OPENING QUESTION.
;THEY WILL SUBSEQUENTLY BE IGNORED BUT WILL BE
;MARKED ON THE TERMINAL ("B") IF SO REQUESTED.
;HEADER ERRORS WHICH ARE DETECTED WITHOUT HEADER
;CRC ERRORS AUTOMATICALLY CAUSE A RESTORE TO BE
;PERFORMED.

;4.0 ERROR REPORTS

;STATUS ERRORS ARE REPORTED BY PRINTING THE CONTENTS
;OF THE MAIN WORKING 8401-3 REGISTERS IN THE FORMAT
;SHOWN BELOW:-

;DS=****** ER=****** CS=****** WC=****** BA=****** TA=****** SA=******

;IF THIS APPEARS AFTER A WRITE TRANSFER, THE ADDRESS
;WILL BE MODIFIED AND A NEW WRITE OPERATION STARTED.
;DATA COMPARISON ERRORS WILL BE REPORTED AS FOLLOWS:-

;DATA ERROR AT TRK**** SECT** WORD******

;        DATA WAS ******  SB ******

; AN "R" AFTER THE REGISTER CONTENTS INDICATES THAT A "RESTORE"
;WAS PERFOMED BEFORE RETRYING THE TRANSFER.
; AN "E" IS PRINTED IF THE TRANSFER IS STILL IN ERROR AFTER
;THE MAXIMUM NUMBER OF RETRIES HAVE BEEN ATTEMPTED.

;IF A STATUS ERROR IS DETECTED DURING A READ TRANSFER,
;NO DATA COMPARISON IS MADE, SINCE IT IS PROBABLE
;THAT THE DATA WORD IN QUESTION WILL BE LOST IN THE
;SILO BUFFER WHEN THE ERROR OCCURRED.
;THE MESSAGE "DONE UPPER (OR LOWER) " IS PRINTED ON COMPLETION
;OF THE APPROPRIATE DISC.

;A MAXIMUM ERROR COUNT OF 128 IS ALLOWED AFTER
;WHICH THE PROGRAM AUTOMATICALLY STOPS.
;LOCATION "ERMAX" MAY BE PATCHED TO ALTER THIS.


;5.0 RUN TIME

;THE PROGRAM TAKES APPROX.  10 MINS TO TEST ONE DISC.

        .TITLE VTLTFP
        .MCALL ..V2..,.EXIT
        ..V2..
        .ASECT
        .NLIST TTM
        .NLIST SEQ
```

```
;TITLE:          8401-3 STATIC TESTS

;PART NUMBER:    -SOURCE: L84-1-DDA-62-11-B1
;                -BINARY: L84-1-DDB-62-11-B1

;WRITTEN:        21/11/77
;LAST MODIFIED:  8/1/80

;1.0 SYSTEM REQUIREMENTS

;       PDP11 SERIES COMPUTER (MIN 8K CORE)
;       8401-3 DISC DRIVE SYSTEM
;       I/O TERMINAL
;       PAPERTAPE READER OR FLOPPY DISC DRIVE


;2.0 PRE-REQUISITES

;BEFORE RUNNING THE DRIVE RELATED TESTS OF THIS PROGRAM,
;  THE DISC SHOULD BE FORMATTED USING THE "HEADER UTILITY PROGRAM"
;PART NUMBER L84-1-DDB-67-11 .


;3.0 OPERATING INSTRUCTIONS

;AFTER LOADING, THE PROGRAM STARTS AT ADDRESS 200.
;THE PROGRAM WILL ASK WHICH UNIT IS TO BE
;TESTED [ 0 OR 1 ].  IF NO DRIVE IS
;CONNECTED AND CONTROLLER ONLY TESTS ARE TO
;BE RUN, TYPE A CAR. RET.
;TYPE "U(PPER)" OR "L(OWER)" FOLLOWED BY A CR
;TO ANSWER WHICH PLATTER IS TO BE TESTED.
```

```
;4.0 TEST DEFINITIONS

;4.1 REGISTER TESTS

;THE REGISTERS ARE FIRST LOADED WITH "ALL
;ONES" AND CHECKED.  A BUS RESET IS THEN ISSUED
;AND THE REGISTERS CHECKED FOR "INITIALIZED"
;STATE.
;EVERY BIT COMBINATION IS LOADED TO EACH REGISTER
;AND CHECKED.

;4.2 INTERRUPT TESTS

;A CHECK IS MADE THAT WITH THE CONTROLLER READY,
;SETTING BIT "IDE" WILL CAUSE AN IMMEDIATE
;INTERRUPT.  THE PROCESSOR PRIORITY LEVEL/S,
;AT WHICH AN INTERRUPT OCCURS, IS REPORTED.

;4.3 SILO TESTS

;THE SILO IS FILLED WITH A PATTERN OF WORDS
;HAVING A DECREMENTING HIGH BYTE AND
;AN INCREMENTING LOW BYTE.
;THE DATA IS THEN READ BACK INTO CORE AND CHECKED
;FOR VALIDITY.
;CHECKS ARE MADE AT KEY STAGES THAT THE SILO STATUS
;FLAGS ARE AS PREDICTED.

;4.4 SECTOR & TRACK ADDRESSING, & OVERFLOW TESTS
;THESE CHECK THAT EVERY VALID SECTOR AND TRACK
;ADDRESS CAN BE ACCESSED AND THAT ALL INVALID ADDRESSES
;UP TO THE MAX.  LOADABLE VALUES CAUSE THE APPROPRIATE
;ERROR BITS TO SET.
;IN ADDITION, A CHECK IS MADE THAT VTSA AND VTTA
;OPERATE CORRECTLY FOR TRANSFERS WHICH OVERFLOW SECTOR
;BOUNDARIES BY ONE WORD.

;4.5 BASIC SEEK AND RESTORE

;A FULL SEEK IN BOTH DIRECTIONS AND A RESTORE IS
;ATTEMPTED AND THE TRACK HEADERS CHECKED FOR
;VALIDITY.

;4.6 ATTENTION INTERRUPT TEST

;A FULL SEEK AND RESTORE IS PERFORMED WITH "AIE"
;BIT SET.  CHECKS ARE MADE THAT THE RIGHT ATTN BIT SETS
;AND THAT ANY INTERRUPT IS VALID.
```

```
;5.0 ERROR REPORTS

;BECAUSE OF THE MANY FUNCTIONS TESTED, ERRORS ARE
;REPORTED BY PRINTING AN ERROR NUMBER WHICH IS
;EFFECTIVELY EXPLAINED BY REFERENCE TO THIS PROGRAM
;LISTING.
;ERRORS OF PARTICULAR SIGNIFICANCE ARE REPORTED
;BY SPECIAL MESSAGES.
;REFER TO THE LISTING FOR DETAILS OF THESE CASES.
;UNEXPECTED ERRORS ARE REPORTED BY PRINTING THE
;CONTENTS OF THE MAIN WORKING REGISTERS.


;6.0 RUN TIME

;THE STATIC TESTS TAKE APPROX. 0.75 MINS TO COMPLETE
;IF NO ERROR MESSAGES ARE PRINTED.
```

C. BOARD 4 JUMPER SELECTION

Board 4 provides the returned write clock to the 5017-3 during a write operation, and this must be phased correctly with respect to the Write Data.

Also, the CRC word generated at the end of the serial write data must be correctly phased to the Returned Write Clock. These requirements are satisfied by wiring the A, B and C jumpers to appropriate positions and are determined during test in the factory. The jumper positions are determined as follows:-

1. Perform a continous write operation using the 'de bug' programme or other simple means.

2. With an oscilloscope, monitor the lines WR DATA (L) and RET WR CLK where they leave the board.

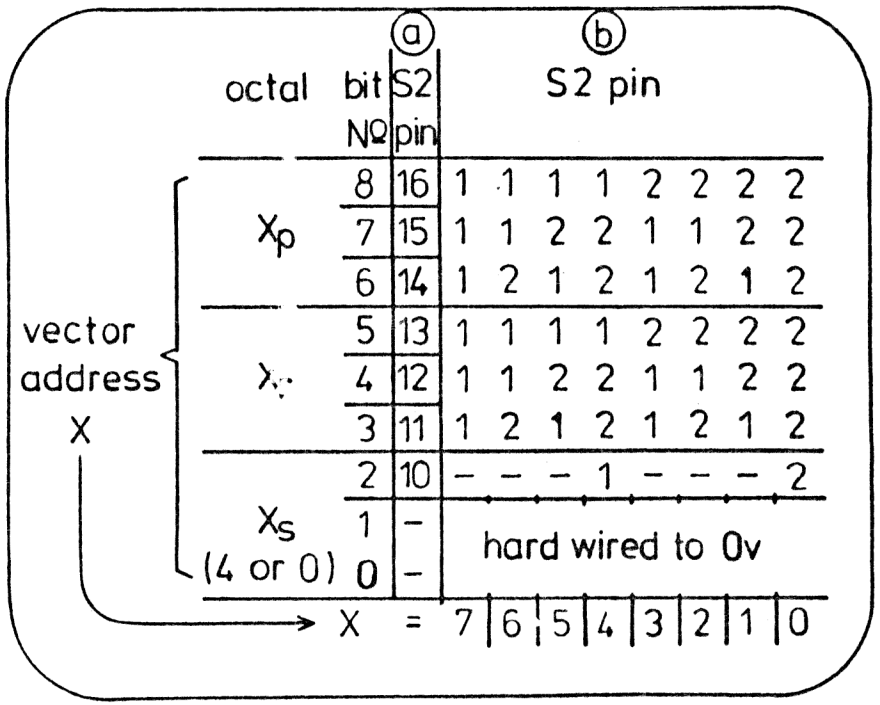
3. Select link A position for nearest coincidence of RET WR CLK positive edge with a WR DATA cell boundary.

4. Move 'scope probes to pins B5-11 and B5-1 (data and CRC clock respectively).

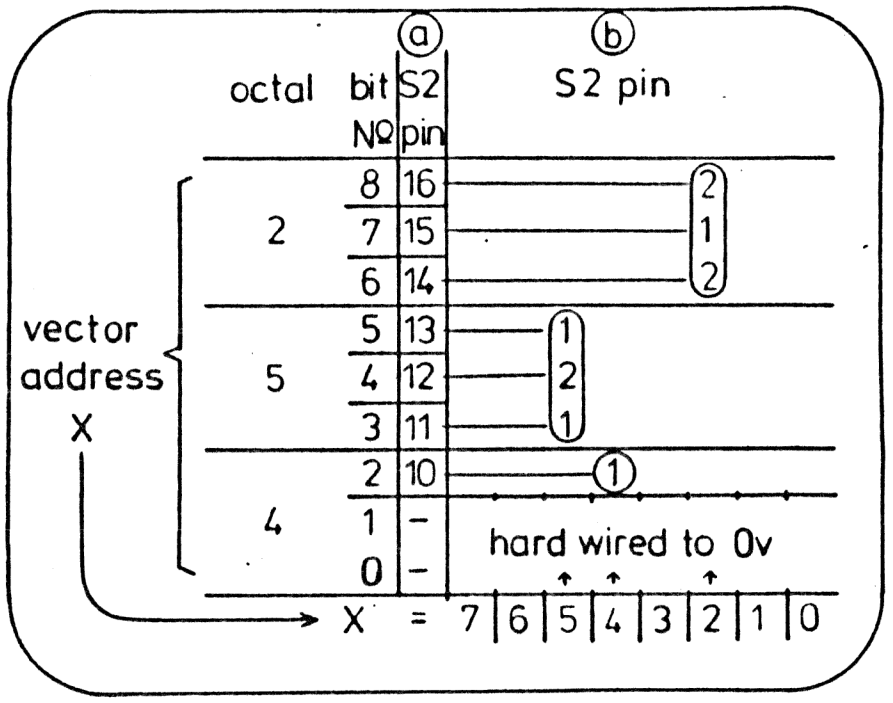
5. Select link B so that first negative clock edge on B5-1, appears just after the start of a write data cell as seen on pin 11.

6. Return 'scope' probes to previous positions as 2.

7. Position link C for best phasing of the CRC word with RET WR CLK. The CRC word may be identified by displaying PARITY GATE, and the phasing requirement is the same as above in paragraph 3.



For required vector address, Xp Xr Xs, connect S2 pins in column (a) to relevant S2 pins in column (b) for various values of X.



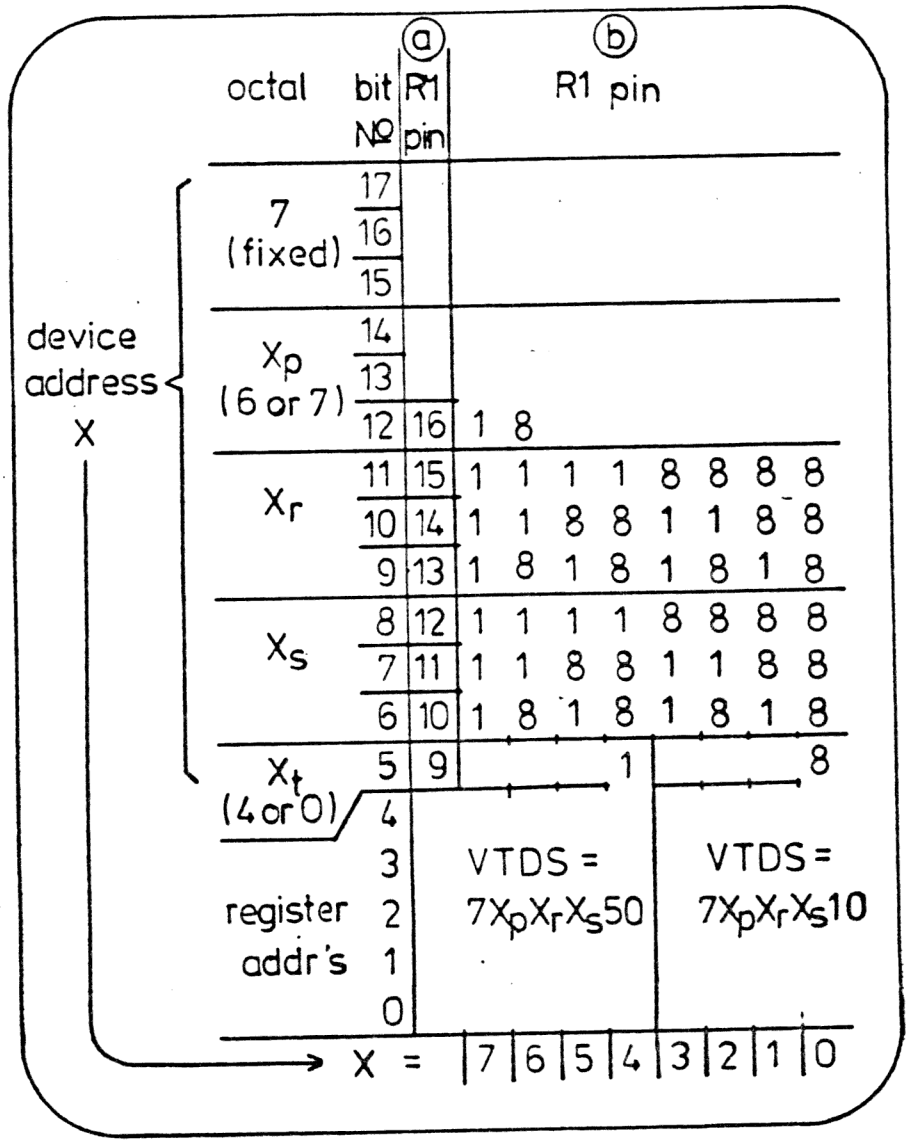
Example:

For vector address 254, connect S2 pins as shown in chart above,

i.e., link S2/1-S2/15 and link S2/2-S2/16
-S2/13 -S2/14
-S2/11 -S2/12
-S2/10

8401-3 VECTOR ADDRESS PATCH
(Header S2, Board 3 L57-A-0204-00)

8401-3 DEVICE ADDRESS PATCH
(Header R1, Board 2 L57-A-0203-00)



For required device address, Xp Xr Xs Xt o, connect R1 pins in column (a) to relevant R1 pins in column (b) for various values of X.

ⓐ T5 pin	ⓑ T5 pin			
14	15	16	1	2
13	4	4	4	9
12	5	5	9	5
11	6	9	6	6
10	9	7	7	7
8	7	6	5	4
priority	4	5	6	7

8401-3 Priority Level Patch
(Header T5, Board L57-A-0204)

For required priority level;- 4, 5, 6 or 7,
link T5 pins under column (a) to relevant
T5 pins under column (b)

For example, for priority level 5, link the following pins:-

14 - 16
13 - 4
12 - 5
11 - 9
10 - 7
8 - 5

1400 SERIES SECTOR FORMAT VS 5010-T DRIVE SECTOR NUMBER

CONTROLLER SECTOR (OCTAL) 1ST REV/2ND REV	DRIVE SECTOR (OCTAL)	DRIVE SECTOR (DECIMAL)
0A	00	01
14B	01	02
0B	02	03
15A	03	04
1A	04	05
15B	05	06
1B	06	07
16A	07	08
2A	10	09
16B	11	10
2B	12	11
17A	13	12
3A	14	13
17B	15	14
3B	16	15
20A	17	16
4A	20	17
20B	21	18
4B	22	19
21A	23	20
5A	24	21
21B	25	22
5B	26	23
22A	27	24
6A	30	25
22B	31	26
6B	32	27
23A	33	28
7A	34	29
23B	35	30
7B	36	31
24A	37	32
10A	40	33
24B	41	34
10B	42	35
25A	43	36
11A	44	37
25B	45	38
11B	46	39
26A	47	40
12A	50	41
26B	51	42
12B	52	43
27A	53	44
13A	54	45
27B	55	46
13B	56	47
30A	57	48
14A	60	49
30B	61	50

PROM TRUTH TABLE FOR L58_M-0715_00 (BOARD 2

WORD	0:	1	1	1	1	1	1	1	1
WORD	1:	0	0	0	0	0	0	0	0
WORD	2:	0	0	0	0	0	0	0	0
WORD	3:	0	0	0	0	0	0	0	0
WORD	4:	0	0	0	0	0	0	1	1
WORD	5:	1	0	0	1	1	1	1	0
WORD	6:	1	1	1	1	1	1	1	0
WORD	7:	1	1	1	1	1	1	1	1
WORD	8:	1	1	1	1	1	1	1	0
WORD	9:	1	1	1	1	1	1	1	1
WORD	10:	0	0	1	1	1	1	1	1
WORD	11:	1	1	1	1	1	1	1	1
WORD	12:	1	0	0	0	0	0	0	0
WORD	13:	1	1	1	1	1	1	1	1
WORD	14:	0	0	0	0	0	0	0	0
WORD	15:	0	0	0	0	0	0	0	0
WORD	16:	0	0	0	0	0	0	0	0
WORD	17:	0	0	0	0	0	0	0	0
WORD	18:	0	0	0	0	0	0	0	0
WORD	19:	0	0	0	0	0	0	0	0
WORD	20:	0	0	0	0	0	0	0	0
WORD	21:	0	0	0	0	0	0	0	0
WORD	22:	0	0	0	0	0	0	0	0
WORD	23:	0	0	0	0	0	0	0	0
WORD	24:	0	0	0	0	0	0	0	0
WORD	25:	0	0	0	0	0	0	0	0
WORD	26:	0	0	0	0	0	0	0	0
WORD	27:	0	0	0	0	0	0	0	0
WORD	28:	0	0	0	0	0	0	0	0
WORD	29:	0	0	0	0	0	0	0	0
WORD	30:	0	0	0	0	0	0	0	0
WORD	31:	0	0	0	0	0	0	0	0

ZERO LINE FILL (1 OF 2)

PROM TRUTH TABLE FOR .... L58-M-0716-00 REV B .... (BOARD 2

WORD	0:	0	0	0	0	0	0	0	1
WORD	1:	0	0	0	0	0	0	0	0
WORD	2:	0	0	0	0	0	0	0	0
WORD	3:	0	0	0	0	0	0	0	0
WORD	4:	1	1	1	1	1	1	1	1
WORD	5:	1	1	1	1	1	1	1	0
WORD	6:	1	1	1	1	1	0	1	1
WORD	7:	1	1	1	1	1	1	1	1
WORD	8:	1	1	1	1	1	1	1	1
WORD	9:	0	0	0	0	1	1	1	1
WORD	10:	0	0	0	0	0	0	0	0
WORD	11:	1	1	1	1	1	1	1	1
WORD	12:	1	1	1	0	0	0	0	0
WORD	13:	1	1	1	1	1	1	1	1
WORD	14:	0	0	0	0	0	0	0	0
WORD	15:	0	0	0	0	0	0	0	0
WORD	16:	0	0	0	0	0	0	0	0
WORD	17:	0	0	0	0	0	0	0	0
WORD	18:	0	0	0	0	0	0	0	0
WORD	19:	0	0	0	0	0	0	0	0
WORD	20:	0	0	0	0	0	0	0	0
WORD	21:	0	0	0	0	0	0	0	0
WORD	22:	0	0	0	0	0	0	0	0
WORD	23:	0	0	0	0	0	0	0	0
WORD	24:	0	0	0	0	0	0	0	0
WORD	25:	0	0	0	0	0	0	0	0
WORD	26:	0	0	0	0	0	0	0	0
WORD	27:	0	0	0	0	0	0	0	0
WORD	28:	0	0	0	0	0	0	0	0
WORD	29:	0	0	0	0	0	0	0	0
WORD	30:	0	0	0	0	0	0	0	0
WORD	31:	0	0	0	0	0	0	0	0

ZERO LINE FILL (2 OF 2)

PROM TRUTH TABLE FOR 158-M-8113-00 (BOARD 1

WORD	0:	0	1	0	0	0	0	0	0
WORD	1:	1	0	0	0	1	1	0	0
WORD	2:	1	0	0	0	0	0	0	0
WORD	3:	0	1	0	0	1	1	0	1
WORD	4:	0	1	0	0	0	0	0	1
WORD	5:	1	0	0	0	1	1	0	1
WORD	6:	1	0	0	0	0	0	0	1
WORD	7:	0	1	0	0	1	1	1	0
WORD	8:	0	1	0	0	0	0	1	0
WORD	9:	1	0	0	0	1	1	1	0
WORD	10:	1	0	0	0	0	0	1	0
WORD	11:	0	1	0	0	1	1	1	1
WORD	12:	0	1	0	0	0	0	1	1
WORD	13:	1	0	0	0	1	1	1	1
WORD	14:	1	0	0	0	0	0	1	1
WORD	15:	0	1	0	1	0	0	0	0
WORD	16:	0	1	0	0	0	1	0	0
WORD	17:	1	0	0	1	0	0	0	0
WORD	18:	1	0	0	0	0	1	0	0
WORD	19:	0	1	0	1	0	0	0	1
WORD	20:	0	1	0	0	0	1	0	1
WORD	21:	1	0	0	1	0	0	0	1
WORD	22:	1	0	0	0	0	1	0	1
WORD	23:	0	1	0	1	0	0	1	0
WORD	24:	0	1	0	0	0	1	1	0
WORD	25:	1	0	0	1	0	0	1	0
WORD	26:	1	0	0	0	0	1	1	0
WORD	27:	0	1	0	1	0	0	1	1
WORD	28:	0	1	0	0	0	1	1	1
WORD	29:	1	0	0	1	0	0	1	1
WORD	30:	1	0	0	0	0	1	1	1
WORD	31:	0	1	0	1	0	1	0	0

SECTOR COUNT (1 OF 2)

PROM TRUTH TABLE FOR ... L58_M_0114_00 REV B ... (BOARD 1

WORD	0:	0	1	0	0	1	0	0	0
WORD	1:	1	0	0	1	0	1	0	0
WORD	2:	1	0	0	0	1	0	0	0
WORD	3:	0	1	0	1	0	1	0	1
WORD	4:	0	1	0	0	1	0	0	1
WORD	5:	1	0	0	1	0	1	0	1
WORD	6:	1	0	0	0	1	0	0	1
WORD	7:	0	1	0	1	0	1	1	0
WORD	8:	0	1	0	0	1	0	1	0
WORD	9:	1	0	0	1	0	1	1	0
WORD	10:	1	0	0	0	1	0	1	0
WORD	11:	0	1	0	1	0	1	1	1
WORD	12:	0	1	0	0	1	0	1	1
WORD	13:	1	0	0	1	0	1	1	1
WORD	14:	1	0	0	0	1	0	1	1
WORD	15:	0	1	0	1	1	0	0	0
WORD	16:	0	1	0	0	1	1	0	0
WORD	17:	1	0	0	1	1	0	0	0
WORD	18:	0	0	1	1	1	1	1	1
WORD	19:	0	0	1	1	1	1	1	1
WORD	20:	0	0	1	1	1	1	1	1
WORD	21:	0	0	1	1	1	1	1	1
WORD	22:	0	0	1	1	1	1	1	1
WORD	23:	0	0	1	1	1	1	1	1
WORD	24:	0	0	1	1	1	1	1	1
WORD	25:	0	0	1	1	1	1	1	1
WORD	26:	0	0	1	1	1	1	1	1
WORD	27:	0	0	1	1	1	1	1	1
WORD	28:	0	0	1	1	1	1	1	1
WORD	29:	0	0	1	1	1	1	1	1
WORD	30:	0	0	1	1	1	1	1	1
WORD	31:	0	0	1	1	1	1	1	1

SECTOR COUNT (2 OF 2)

Register Symbol	Standard Address	Bit Nº 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VTDS	776710	unit ready	unit on line		hdr. err.	act. addr. err.	seek in prog.	unit unsafe	write prot'd	ø	ø	ø	ø	ø	ø	attn. 1	attn. ø
VTER	776712	write prot. err.	insafe err.	bad sect. det'd	non exist track	non exist sect.	prog. err.	hdr. CRC err.	ø	data CRC err.	ø	ø	xfer err.	wrchk err.	non exist mem.	end of pack	ø
VTCS	776714	error	set sect. prot.	attn. int. enabl	read all	set bad sect.	ø	unit sel.	platt sel.	ready	ready int. enabl	mem. ext. 1	mem. ext. ø	funct 2	funct 1	funct ø	go
VTWC	776716																
VTBA	776720																
VTTA	776722	ø	ø	ø	ø												
VTSA	776724	ø	ø ← current RAISED.			sector		address →		ø	ø	← desired			sector		address →
VTSILO	776726																
VTMNT	776730	silo i/p ready	sect. hdr. err.	track hdr. err.						silo o/p ready							
VTDWC	776732																

	4	3	2	1	0
CLEAR STS	0	0	0	0	1
WRITE	0	0	0	1	1
READ	0	0	1	0	1
WRITE CHECK	0	0	1	1	1
SEEK	0	1	0	0	1
WRITE HEADER	0	1	0	1	1
RESTORE	0	1	1	0	1
READ HEADER	0	1	1	1	1

code	function
1	system clear
3	write
5	read
7	write check
11	seek
13	write header
15	restore
17	read header

3rd ANGLE PROJECTION B.S 308

'UNIBUS' IN

BOARD 1 (L57-A-0202-00)

BOARD 2 (L57-A-0203-00)

BOARD 3 (L57-A-0204-00)

BOARD 4 (L57-A-0205-00)

'UNIBUS' OUT OR TERMINATOR CARD

'UNIBUS' is a trademark of the Digital Equipment Corporation.

SA REG, SA OUT, NON EXIST SECTOR, TA REG, TA OUT, NON EXIST TRACK, ER OUT, ERRORS, SA OUT, CLIENT DRIVE SECTOR, SECTOR COMP, SECTOR INTERLACE, HEADER GENERATOR, BUS OUT DRIVERS, TAG GENERATOR, STROBE, SERIAL HEADER DATA, SECTORS EQUAL, BOARD 4, SEEK RESTORE, TAS 1,2&3

MISC. CONTROL, MSYN, INIT, CI, SSYN, DEVICE ADDRESS DECODE, ZERO LINE FILL, 18 ADDRESS LINES IN, 18 ADDRESS LINES OUT, 16 DATA LINES IN/OUT, REG. ADDR. DECODE, DS, ER, CS, WC, BA, TA, SA, SILO, MNT, DWC

WC OUT, WC REG., CS OUT, CS REG., BA REG., BA OUT, FUNC'N DECODE, WRITE, READ, WRITE CHECK, CLEAR, ID TRANSFER CONTROL, UNIT sel, ERROR, ER OUT

INTERNAL TRISTATE DATA BUS (DB0-DB15)

TRANSMITTERS / RECEIVERS

CP-2, CP-1

CONTROL CABLE (L16-S-0300-TAB)

DATA CLOCK CABLE 'A' (L16-S-0299-TAB)

DAISY CHAIN CONTROL CABLE (L16-S-0301-TAB)

DATA CLOCK CABLE 'B' (L16-S-0299-TAB)

TERMINATOR (L57-A-0166-00)

DP-8, DP-10, DP-9

DISC DRIVE UNIT 'A' (L34-A-0106-TAB)

DISC DRIVE UNIT 'B' (L34-A-0106-TAB)

BG4-BG7, BG4-BG7, BR4-BR7, INTR, PRIORITY LEVEL, BG, BR, INTERRUPT LOGIC, VECTOR ADDRESS, ERRORS, ATTENTION, READY, SSYN, SACK, BBSY, MSYN, DMA LOGIC

DWC OUT, DWC REG, BUFFER CONTROL LOGIC, BUS I/P BUFF, SILO BLOCK, BUS O/P BUFF, DRIVE TRANSFER START/STOP, ATTENTION, DS OUT, ATTENTN LOGIC, MASTER CLOCK, READ/WRITE CLOCK, RETURN WRITE CLOCK, SERIAL WRITE DATA, SERIAL READ DATA

BOARD 1 SECTORS EQUAL, R/W CLOCK, BIT/BYTE COUNTR, DRIVE TRANSFER CONTROL, R/W CLOCK DELAY, HEADER CHECK, WRITE CHECK, HEADER ERROR, WRITE CHK ERROR, DRIVE I/P BUFF, SER/DES., DRIVE O/P BUFF, CRC GENERATOR, CRC ERROR

ABBREVIATIONS

DS	DRIVE STATUS REGISTER
ER	ERROR REGISTER
CS	CONTROL & STATUS REGISTER
WC	WORD COUNT REGISTER
BA	BUS ADDRESS REGISTER
TA	TRACK ADDRESS REGISTER
SA	SECTOR ADDRESS REGISTER
SILO	SILO BUFFER
MNT	MAINTENANCE REGISTER
DWC	DRIVE WORD COUNT REGISTER
CRC	CYCLIC REDUNDANCY CHECK
DMA	DIRECT MEMORY ACCESS
SER/DES	SERIALISER / DESERIALISER

→ WRITE DATA

← READ DATA

NOTES

1) For single Drive working, remove DATA CLOCK CABLE 'B' and DAISY CHAIN CABLE. Connect TERMINATOR to DP9 of UNIT 'A'

REV	CHKD.	DATE	MOD.No.
A1		26-2-79	
A			

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES(INCHES):- FRACTION ± 1/64
.XX± .010 .XXX± .005
TOLERANCE(mm) X: ± .50 .XX: ± .10
ANGULAR ± 0° 30' REMOVE SHARP EDGES
SURFACE ROUGHNESS 125 √

FIRST USED ON

MATERIAL

FINISH

DRN.	A. MASON	DATE 6-2-79
CHKD	R. WATSON	DATE

Vermont Research

TITLE 8401-3
SYSTEM ARRANGEMENT
BLOCK DIAGRAM

SIZE L | NUMBER I-0142

SCALE | SHEET 1 OF 1